

MAINTENANCE MANUAL

Model 680-01

Arbitrary Waveform Generator

© 1990 Wavetek

This document contains information proprietary to Wavetek and is provided solely for instrument operation and maintenance. The information in this document may not be duplicated in any manner without the prior approval in writing from Wavetek.

WAVETEK

WAVETEK is a trademark of
Wavetek Wandel-Gottmann, Inc.
(WWG) and is used by Fluke under a
transitional license agreement. Fluke
is not affiliated with WWG.

WAVETEK SAN DIEGO, INC.
9045 Balboa Ave., San Diego, CA 92123
P. O. Box 85265, San Diego, CA 92138
Tel 619/279-2200 TWX 910/335-2007

Manual Revision 3/90
Manual Part Number: 1300-00-0546-1
Instrument Part Number: 1000-00-0546

WARRANTY

Wavetek warrants that all products manufactured by Wavetek conform to published Wavetek specifications and are free from defects in materials and workmanship for a period of one (1) year from the date of delivery when used under normal conditions and within the service conditions for which they were furnished.

The obligation of Wavetek arising from a Warranty claim shall be limited to repairing, or at its option, replacing without charge, any product which in Wavetek's sole opinion proves to be defective within the scope of the Warranty. In the event Wavetek is not able to modify, repair or replace non-conforming defective parts or components to a condition as warranted within a reasonable time after receipt thereof, Buyers shall be credited for their value at the original purchase price.

Wavetek must be notified in writing of the defect or nonconformity within the Warranty period and the affected product returned to Wavetek's factory or to an authorized service center within (30) days after discovery of such defect or nonconformity.

For product warranties requiring return to Wavetek, products must be returned to a service facility designated by Wavetek. Buyer shall prepay shipping charges, taxes, duties and insurance for products returned to Wavetek for warranty service. Except for products returned to Buyer from another country, Wavetek shall pay for return of products to Buyer.

Wavetek shall have no responsibility hereunder for any defect or damage caused by improper storage, improper installation, unauthorized modification, misuse, neglect, inadequate maintenance, accident or for any product which has been repaired or altered by anyone other than Wavetek or its authorized representative and not in accordance with instructions furnished by Wavetek.

Exclusion of Other Warranties

The Warranty described above is Buyer's sole and exclusive remedy and no other warranty, whether written or oral, is expressed or implied. Wavetek specifically disclaims the implied warranties of merchantability and fitness for a particular purpose. No statement, representation, agreement, or understanding, oral or written, made by an agent, distributor, representative, or employee of Wavetek, which is not contained in the foregoing Warranty will be binding upon Wavetek, unless made in writing and executed by an authorized Wavetek employee. **Under no circumstances shall Wavetek be liable for any direct, indirect, special, incidental, or consequential damages, expenses, losses or delays (including loss of profits) based on contract, tort, or any other legal theory.**

680 Manual Set

680 Standard Manuals

	Operator's			Maintenance				
	General Description	Installation	Operation	Theory of Op	Calibration	Troubleshooting	Schematics	Parts Lists
Mainframe	Mainframe Operator's Manual			Mainframe Maintenance Manual				
Arb Gen	Arb Operator's Manual			Arb Maintenance Manual				
Timing Gen	TGen Operator's Manual			TGen Maintenance Manual				
Pulse Gen	PGen Operator's Manual			PGen Maintenance Manual				
DMM	DMM Instruction Manual							
Counter	1993 Counter InstructionManual							

680 MATE Manuals

	Operator's			Maintenance				
	General Description	Installation	Operation	Theory of Op	Calibration	Troubleshooting	Schematics	Parts Lists
Mainframe	Mainframe Operator's Manual			Mainframe Maintenance Manual				
Arb Gen	Arb Operator's Manual			Arb Maintenance Manual				
Timing Gen	TGen Operator's Manual			TGen Maintenance Manual				
Pulse Gen	PGen Operator's Manual			PGen Maintenance Manual				
DMM	(Contained In Standard DMM Instruction Manual)							
Counter	(Contained in Standard 1993 Counter Instruction Manual)							



Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_11289

CONTENTS

SECTION 1 GENERAL DESCRIPTION

1.1	GENERAL DESCRIPTION (Model 680-01)	1-1
1.2	CAPABILITIES	1-1
1.3	SPECIFICATIONS	1-2
1.3.1	Arbitrary Characteristics	1-2
1.3.2	Functions	1-2
1.3.3	Frequency	1-2
1.3.4	Amplitude	1-3
1.3.5	Offset	1-3
1.3.6	DC Voltage Accuracy	1-3
1.3.7	Outputs	1-3
1.3.8	Inputs	1-3
1.3.9	Internal I/O	1-3
1.3.10	General	1-3

SECTION 2 THEORY OF OPERATION

2.1	INTRODUCTION	2-1
2.2	WAVETEK MODEL 680-01 INTERFACE, BUSES AND GENERAL DESCRIPTION	2-2
2.2.1	VME Bus Interface	2-2
2.2.2	Timing Bus Interface	2-2
2.2.3	Trigger Control and Selector	2-2
2.2.4	Clock Control and Selector	2-4
2.2.5	Digital Waveform Synthesizer (Arb Memory Board)	2-4
2.2.6	Waveform DAC and Preamp	2-4
2.2.7	Filter	2-5
2.2.8	Output Amplifier and Attenuators	2-5
2.2.9	Sync Buffers	2-5
2.2.10	Output Protection	2-5
2.2.11	Calibration Bus Interface	2-5
2.2.12	Analog Bus Interface	2-5
2.2.13	DAC Bus	2-5
2.2.14	Power Distribution Bus and Interface	2-5
2.3	FUNCTIONAL BLOCK DIAGRAM DESCRIPTION	2-5
2.3.1	VME Bus Interface	2-6
2.3.2	Local Data Latches	2-6
2.3.3	Arb Operating System ROM	2-6
2.3.4	Trigger/Clock Input Conditioning	2-6
2.3.5	Timing Interface	2-6
2.3.6	Trigger Control Logic	2-6
2.3.7	Internal Clock	2-9
2.3.8	Clock Multiplexer	2-9
2.3.9	Digital Waveform Synthesizer (Arb Memory Board)	2-10
2.3.9.1	Memory Address Generator	2-10
2.3.9.2	Memory Control Registers	2-11
2.3.9.3	Waveform Memory	2-11

CONTENTS (Continued)

2.3.10	Waveform Data Buffer	2-12
2.3.11	Waveform DAC	2-12
2.3.12	Preamp	2-12
2.3.13	100KHz/4MHz Filter	2-12
2.3.14	4-Bit Binary Attenuator	2-12
2.3.15	Output Amplifier	2-12
2.3.16	20dB/40dB Attenuator and Impedance Selector	2-12
2.3.17	Output Protection	2-12
2.3.18	Calibration Interface	2-12
2.3.19	Analog Interface	2-14
2.3.20	Sync Buffers	2-14
2.4	AUTOMATIC DIAGNOSTICS and CALIBRATION	2-15
2.4.1	Self Test	2-15
2.4.2	Auto Cal	2-15

SECTION 3 CALIBRATION

3.1	INTRODUCTION	3-1
3.2	MANUAL CALIBRATION PROCEDURE	3-1
3.3	AUTO CALIBRATION PROCEDURE	3-2

SECTION 4 TROUBLESHOOTING

4.1	INTRODUCTION	4-1
4.2	NO MODULE ID	4-2
4.3	NO OUTPUT IN CONTINUOUS MODE	4-2
4.4	NO OUTPUT IN THE TRIGGERED MODE	4-2
4.5	NO WVFM SYNC OUTPUT	4-3
4.6	NO ARB SYNC OUTPUT	4-3
4.7	HOW TO DECODE A SELF TEST FAILURE	4-4
4.7.1	Programming	4-4
4.7.2	Status	4-4
4.8	HOW TO DECODE AN AUTO CAL FAILURE	4-4
4.8.1	Programming	4-4
4.8.2	Status	4-5
4.9	HOW TO DECODE A GLOBAL AUTO CAL AND SELF TEST STATUS	4-5

SECTION 5 SCHEMATICS AND PARTS LIST

5.1	DRAWINGS	5-1
5.2	ERRATA	5-1
5.3	ORDERING PARTS	5-1

ILLUSTRATIONS

2-1	Generic Waveform Generator	2-3
2-2	Wavetek Model 680-01 Arbitrary Waveform Generator	2-3
2-3	Digital Waveform Synthesizer (Arb Memory Board)	2-4
2-4	Model 680-01 Functional Block Diagram	2-7
2-5	Trigger Clock Conditioning	2-8
2-6	Phase Locked Loop Internal Clock.....	2-9
2-7	Arbitrary Waveform Address Generator	2-11
2-8	Self Test Flow Chart	2-16
2-9	Auto Cal Flow Chart	2-17
3-1	Waveform Specification	3-1
3-2	Calibration of the Arbitrary Waveform Generator	3-2
4-1	Wavetek Arbitrary Waveform Generator	4-1

TABLES

1-1	Arbitrary Waveform Generator Capabilities	1-1
2-1	VME Interface Functions	2-3
2-2	Quad Threshold DAC Selector	2-6
2-3	Trigger Control Logic I/O Selector	2-8
2-4	Clock Multiplexer Input Selection	2-10
2-5	Relay Function Summary	2-13
2-6	Calibration Multiplexer Input	2-14
2-7	Self Test Status Decoding	2-15
3-1	Manual Calibration Test Equipment	3-1
3-2	Aberration Specification	3-1
3-3	Calibration Status	3-2
4-1	Equipment Required	4-1
4-2	Self Test Status Decoding	4-4
4-3	Global Auto Cal and Self Test Status	4-5

SAFETY FIRST



PROTECT YOURSELF. Follow these precautions:

- Don't touch the outputs of the instrument or any exposed test wiring carrying the output signals. This instrument can generate hazardous voltages and currents.
- Don't bypass the power cord's ground lead with two-wire extension cords or plug adaptors.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the power receptacle to the chassis ground terminal (marked with  or ).
- Don't hold your eyes extremely close to an rf output for a long time. The normally nonhazardous low-power rf energy generated by the instrument could possibly cause eye injury.
- Don't plug in the power cord until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the **CAUTION** statements. They point out situations that can cause equipment damage.

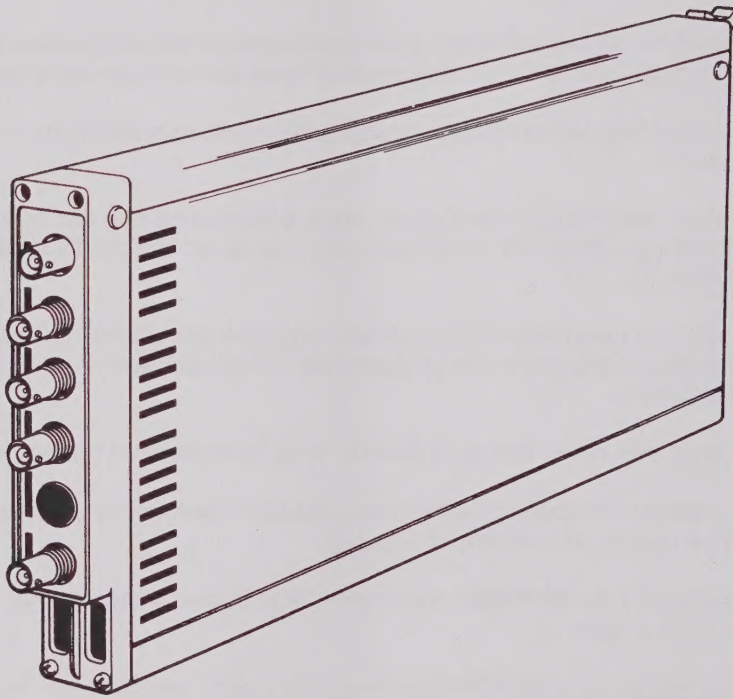


Figure 1-1. Wavetek Arbitrary Waveform Generator

1

SECTION INTRODUCTION

1.1 GENERAL DESCRIPTION (MODEL 680-01)

Model 680-01, 20 MHz Arbitrary Waveform Generator (Arb), seen in figure 1-1, generates arbitrary waveforms with up to 12 bits of vertical resolution and 12K horizontal resolution, function generator waveforms of Sine, Triangle, Ramp, Square, DC, and their inverse. These

function generator waveforms are permanently stored in ROM. Operating modes include: Continuous, Triggered, Gated, and Burst.

1.2 CAPABILITIES

The Arbitrary Waveform Generator programming capabilities are shown in table 1-1.

Table 1-1. Arbitrary Waveform Generator Capabilities

Category	Capability	Description
Arbitrary Waveforms	Ten Waveforms	Up to ten arbitrarily defined waveforms can be stored. The user defines the waveform length and shape.
Standard waveforms	Five types	Sine, Square, Triangle, Ramp, and DC signals can be generated. The polarity and number of repetitions can be selected.
Waveform Controls	Timing	The output waveform frequency, clock source and the number of times a waveform is to be repeated are programmable.
	Filtering	The output waveform can be filtered, if desired. The user may select low pass filtering at 0.1 MHz or at 4.0 MHz.
	Levels	The output voltage levels can be user defined.
	Waveshape	User programmable.
	Duty Cycle	The Ramp and Square wave signals from the standard function generator may be programmed for variable duty cycles.
	ON/OFF Control	The ARB OUT output can be turned ON or OFF by a control relay.
	Impedance Adjust	A user defined value can be selected. The module can also measure the attached load impedance and set the internal impedance.
Output Modes	Summing	The output signal of the Arbitrary Waveform Generator may be summed to the system Analog Sum Bus, ANASUM; ANASUM can be summed to the Arbitrary Waveform Generator output, or summing can be disabled.
	Continuous	Output waveforms can be generated continuously.
	Triggered	A single cycle of a user selected waveform can be generated on the event of a valid selected trigger. The Model 680 System Trigger (STRIG), the external trigger (TRIG IN), or the Model 680 System Sync signal (SSYNC) are selectable trigger sources.
	Gated	The user selected waveform may be generated continuously when the trigger input is a logic high.

Table 1-1. Arbitrary Waveform Generator Capabilities (Cont'd)

Category	Capability	Description
ARB Output (BNC Connector)	Burst Arbitrary Waveform Generator signal output	A waveform can be generated a programmable number of times. This output generates a synchronization pulse at the beginning of each waveform period.
WVFMSSync Output (BNC Connector)	Arbitrary Waveform Generator sync output	This output generates a synchronization pulse at the beginning of each waveform period. The Sync pulse becomes positive going at the positive zero crossing point of the output waveform and negative going at the negative zero crossing point.
Arbsync Output (BNC Connector)	Arbitrary Waveform Generator sync output	This output can be programmed to generate synchronization pulses at any point(s) within a user defined (arbitrary) waveform.
Clock In (BNC Connector)	Clocking from an external source	An external clock can be selected instead of the internally generated clock, permitting exact synchronization of user generated (arbitrary) waveforms with external sources.
Trig In (BNC Connector)	Triggering from an external source	This trigger input can be used to trigger events inside the Arbitrary Waveform Generator.
Miscellaneous module inputs	System synchronization Amplitude Modulation	A synchronization pulse can be generated to the SSYNC bus at the beginning of each waveform or at any desired point(s) of a user defined (arbitrary) waveform. This feature can be disabled so no synchronization pulses are generated at any time. Any timing generator installed in the Model 680 main frame can be amplitude modulated by the output of an adjacent Arbitrary Waveform Generator.

1.3 SPECIFICATIONS

1.3.1 Arbitrary Characteristics

Horizontal Resolution: 12K points.

Vertical Resolution: 12 bits (-2047 to 2047).

Waveform Memory: Stores up to 10 waveforms with user defined length from 8 points to memory maximum.

Arb Clock:

Sampling Frequency: 1 mHz to 20 MHz.

Resolution: 4 digits or 1 mHz.

Waveform Repetition Rate: 2.5 MHz (clock divided by the number of waveform points).

Accuracy: 5 ppm.

Stability: 2 ppm in 10 min., $\pm 3^{\circ}\text{C}$.

1.3.2 Functions

Function Generator Mode: Sine, Triangle, Ramp, Square, DC, and their inverse.

Arbitrary Generator Mode: Sin(X), Cos(X), Exp(X), Sin(X)/X and user defined.

Operational Modes: Continuous, Triggered, Gated, and Burst.

Burst: Programmable from 1 to 65,535.

Sine Distortion:

10 μHz to 99.9 kHz: <0.2%.

To 100 kHz: <0.7%.

No harmonics above -40dBc 100kHz to 4 Mhz.

Square Transition Time: (50 Ω into 50 Ω) <25 ns.

Square Aberrations:

<10 Vp-p: $\pm(5\% + 20 \text{ mV})$.

>10 Vp-p: $\pm(10\% + 20 \text{ mV})$.

Duty Cycle: (Square and Ramp) 0.1% to 99.9%. Square defaults to 50% above 1 MHz.

1.3.3 Frequency

Range

Sine: 10 mHz to 4 MHz.

Square: 10 mHz to 10 MHz.

Triangle/Ramp: 10 mHz to 250 kHz.

Resolution: 4 digits or 10 mHz.

1.3.4 Amplitude

Range: 10 mVp-p to 20 Vp-p into a 50Ω load.

Resolution: 1 mV to 10 mV depending upon range.

Accuracy (Into 50Ω, 0.1% load).

10 to 20 Vp-p: $\pm(1\% \text{ of programmed value} + 5\text{mV})$.

1 to 10 Vp-p: $\pm(1\% + 5\text{mV})$.

0.1 to 1 Vp-p: $\pm(2\% + 2\text{mV})$.

10 to 100 mVp-p: $\pm(3\% + 0.5 \text{ mV})$.

Frequency Response

Range	Response	Filter Setting
100 μHz to 9.999 kHz	$\pm 1\%$	100 kHz
10 kHz to 49.999 kHz	$\pm 3\%$	100 kHz
50 kHz to 0.9999 MHz	$\pm 5\%$	4 MHz
1 MHz to 4 MHz	$\pm 10\%$	4 MHz

1.3.5 Offset

Range

For given offset range, minimum amplitude must be:

Offset	Minimum Amplitude (Vp-p)
5.001 to 10 Vdc	>0.52
0.501 to 5 Vdc	>0.25
51 to 500 mVdc	>0.026
5 to 50 mVdc	>0.002

Programmable Load Impedance

(Enter mode. This applies to use of loads other than 50Ω)

Range: 25 to 1kΩ.

Accuracy: $\pm 5\%$.

1.3.6 DC Voltage Accuracy

DC Function Accuracy (Into 50Ω, 0.1% load).

5.001 to 10 Vdc: $\pm(1\% + 40 \text{ mV})$.

0.501 to 5 Vdc: $\pm(1\% + 40 \text{ mV})$.

51 to 500 mVdc: $\pm(2\% + 10 \text{ mV})$.

5 to 50 mVdc: $\pm(3\% + 3 \text{ mV})$.

Resolution: 1 mV from lowest to highest range.

1.3.7 Outputs

Function Output, Waveform Sync Output, and Arbitrary Sync Output.

1.3.8 Inputs

Trigger Input and External Clock Input.

1.3.9 Internal I/O

System Trigger Bus, System Sync Bus, Analog Summing Bus, Pulse Amplitude Modulation (PAM source for timing generator).

1.3.10 General

Stored Settings: Provided by Model 680 Main Frame. There are 99 stored settings that can be divided between the main frame and the modules to meet user needs.

Environment: Refer to Model 680 Main Frame specifications.

Dimensions: 15.9 cm (6.25 in.) high, 41.9 cm (16.5 in.) long, 3.0 (1.2 in.) wide.

Weight: 1.8 kg (4 lb) net.

Power: Less than 32 W.

2

SECTION

THEORY OF OPERATION

2.1 INTRODUCTION

To operate, the Wavetek Model 680-01 Arbitrary Waveform Generator module (Arb) requires installation in a Model 680 Mainframe. Section 2 discusses the Model 680 Mainframe interface, and the block diagram description of the 20 MHz Arbitrary Waveform Generator module.

Under control of the Model 680 Mainframe resources, the Model 680-01 Arbitrary Waveform Generator:

- Generates both arbitrarily defined waveforms and standard function generator waveforms at the Arb Out BNC connector on the rear panel of the module.
- Generates synchronization pulses at the Arb Sync output BNC connector; the number of pulses per period and phase relationship of these pulses are user programmable.
- Generates a synchronization pulse at the WVFM Sync BNC connector once for each output period.
- Can be programmed to algebraically sum the module output (Arb Out) to the Model 680 Mainframe Analog Bus Analog Sum (ANASUM) signal or sum ANASUM to the Arb Output.
- Can be programmed to generate synchronization pulses to the Model 680 Mainframe Timing Bus System Trigger (STRIG) or System Sync (SSYNC) lines.
- Can be programmed to amplitude modulate the output of an adjacent Timing Generator located in the next higher even numbered slot.

The Arbitrary Waveform Generator relies on the Model 680 Mainframe for:

- Operating power.
- The 10 MHz reference frequency.
- The System Trigger (STRIG) line as a signal path for intermodule trigger signals.
- The System Sync (SSYNC) line as a signal path for intermodule synchronization signals.

- The Analog Sum (ANASUM) line as a signal path for intermodule analog summing features.
- The VME Bus for control signals that supervise the entire operation of the Arbitrary Waveform Generator.
- The GPIB and front panel interfaces that allow user operation of the module.
- The Ref/Cal board for automatic calibration and diagnostics.
- Signal connections to adjacent modules that allow amplitude modulation features.
- Retention of correction factor data obtained during the module's automatic calibration cycle.

The Generic Arbitrary Waveform Generator Description

The generation of arbitrary waveforms requires a sequential definition of the waveform amplitude vs time. This is normally accomplished by storage of binary numbers in Random Access Memory. The waveform may be pre-defined (stored in Read Only Memory) or operator defined. Operator defined waveforms require the operator to enter the waveform amplitude for each given time selected. There is a minimum number of values needed for any given waveform definition and the memory size determines the maximum number of values that can be entered.

The Digital to Analog Converter (DAC) converts the binary numbers to a series of discrete voltage values. The more bits per binary number, the greater the accuracy of the voltage (12 bits, for example, would permit 4096 discrete values between 0% and 100% of full scale value). The more binary numbers per waveform, the better the definition of the waveshape (a triangle wave, for example, can be defined by three points, but a sine wave requires a greater number). Time penalties are imposed as the accuracy increases and the shape is better defined. The more bits per number, the longer it takes to convert to an analog voltage; the more numbers per waveform, for any given frequency, the faster they must be retrieved from memory and the faster the DAC

must convert them; each requires a memory size increase. Refer to Figure 2-1.

Logic circuits typically detect the beginning address of the waveform memory and generate a sync pulse to coincide with the start of the period.

Unless a stepped or pulse waveform is desired, a "reconstruction filter" must be used on waveshapes defined by only a few points. An enlarged view of the waveform out of the DAC will show discrete steps instead of a smooth line. The filter accomplishes two basic jobs; it smooths the waveform by filling the steps and it also suppresses harmonics of the primary frequency that would otherwise be seen at the output (stepped abrupt changes generate harmonics). Often a preamp is placed between the DAC output and the filter input both for voltage/current gain and isolation.

The Output Amplifier provides the necessary current and voltage gain to deliver the maximum selected amplitude to the designated load.

The Microprocessor control is transparent. An arbitrary waveform generator is extremely dependant on extensive, high speed control which can only be supplied by a microprocessor. By acting on the operator requests, the microprocessor and software retrieve memory data and adjust the hardware as necessary to yield the desired output.

2.2 WAVETEK MODEL 680-01 INTERFACE, BUSES AND GENERAL DESCRIPTION

Figure 2-2 shows the Wavetek Model 680-01 Arbitrary Waveform Generator simplified block diagram. Use figure 2-2 and the detailed block diagrams found throughout this section to see the interconnection of the module functional blocks and the interface with the Model 680 Mainframe.

2.2.1 VME Bus Interface

The VME I/O buffers, data latches, address decoder, control registers and module firmware are controlled by the VME Microprocessor Board on the Model 680 Mainframe and control all operations of the Arbitrary Waveform Generator. The interrupt functions are not programmed to be active.

Table 2-1 lists each section and its function.

2.2.2 Timing Bus Interface

The Timing Bus carries trigger and clock signals in both directions. The Arbitrary Waveform Generator may use the trigger or sync signals generated by the Model 680 Mainframe, or provide a trigger/sync for use by the

mainframe. Three of the bi-directional Timing Bus clock signals are available with buffers in the interface, however, only one of them is currently used by the Arbitrary Waveform Generator. The 10 MHz master reference frequency generated in the Model 680 Mainframe is buffered through the Timing Bus Interface for use by the Arb.

Table 2-1. VME Interface Functions

SECTION	FUNCTION
VME I/O Buffers	Buffers the VME Bus address lines, VME Bus interrupt interface signals, and the VME Bus Control Signals.
Data Latches	Latches the VME Bus Data lines.
Main Address Decoder	Decodes the VME Bus signals and selects the addressed control registers of the Arbitrary Waveform Generator.
Control Registers	Latches control bits from the Local Data Bus when selected by the Main Address Decoder.
Module Firmware	These ROMs contain instructions for the VME Microprocessor board that implement control of the Arb.

2.2.3 Trigger Control and Selector

The Trigger Control and Selection determines which one of the four trigger sources listed below is to be used for the Trigger at the Digital Waveform Synthesizer:

- 1. The external trigger from the Ext Trig BNC
- 2. The signal appearing on the System Trigger line
- 3. The signal appearing on the System Sync line
- 4. The Manual Trigger signal decoded from a VME Bus Interface data signal.

The Trigger Control and Selector has both a variable threshold and a slope control for the External Trigger. It

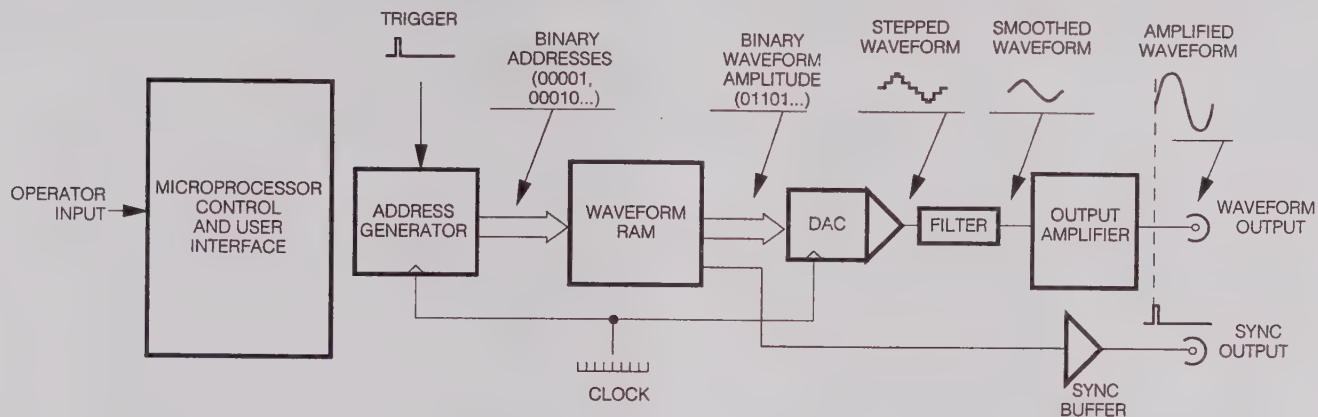


Figure 2-1 Generic Arbitrary Waveform Generator

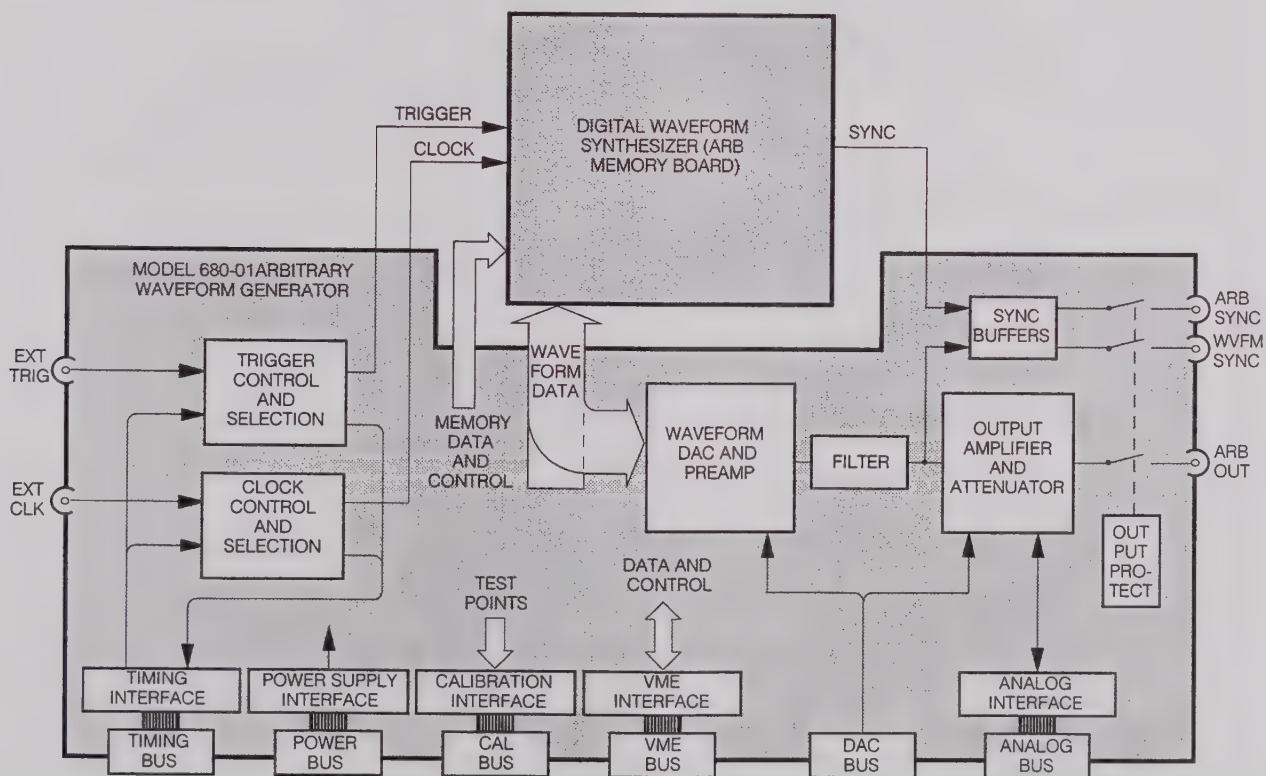


Fig. 2-2 Wavetek Model 680-01 Arbitrary Waveform Generator

also is responsible for directing one of the two sync signals generated by the Arb to the Timing Bus Interface for use by the Model 680 Mainframe on either the System Trigger line or the System Sync line.

2.2.4 Clock Control and Selector

The Clock Control and Selector determines which one of the four clock sources listed below is to be used for the Waveform Clock signal:

1. The external clock signal from the Ext Clk BNC
2. The signal generated by the Arb internal clock
3. The signal appearing on the TTL19 line
4. The 10 MHz master reference.

The Clock Control and Selector provides the external clock signal with a variable threshold control, developed from VME Bus Interface control signals.

Using VME Interface control signals, the internal clock frequency is automatically programmed to provide the correct output waveform frequency from the number of steps stored in memory.

The Clock Control and Selector also selects the same clock signal for the waveform digital to analog conversion (DAC) clock that has been selected for use as the waveform memory (RAM) clock.

When requested, the Clock Control and Selector will provide a selected clock signal to the Model 680 Mainframe over the Timing Bus.

2.2.5 Digital Waveform Synthesizer (Arb Memory Board)

All parts of the Digital Waveform Synthesizer are located on the Arb Memory Board. The Arb Memory Board is a sub-assembly of the Arbitrary Waveform Generator module.

The Digital Waveform Synthesizer controls the retrieval of binary data from the Waveform RAM, located on the Arb Memory Board. Waveform generation takes place as the Address Generator, generating sequential addresses, extracts binary values from Waveform RAM at each occurrence of the Waveform Clock; simultaneously these data are converted into analog voltages at the Waveform DAC located on the Arb Generator Board at each occurrence of the DAC Clock.

The retrieved waveform data is 14 bits wide; 12 bits, 0 through 11, are converted to analog voltages by the waveform DAC while bits 12 and 13 are sync signals. Refer to Figure 2-3.

2.2.6 Waveform DAC and Preamp

The Waveform DAC converts the 12-bit stream of binary

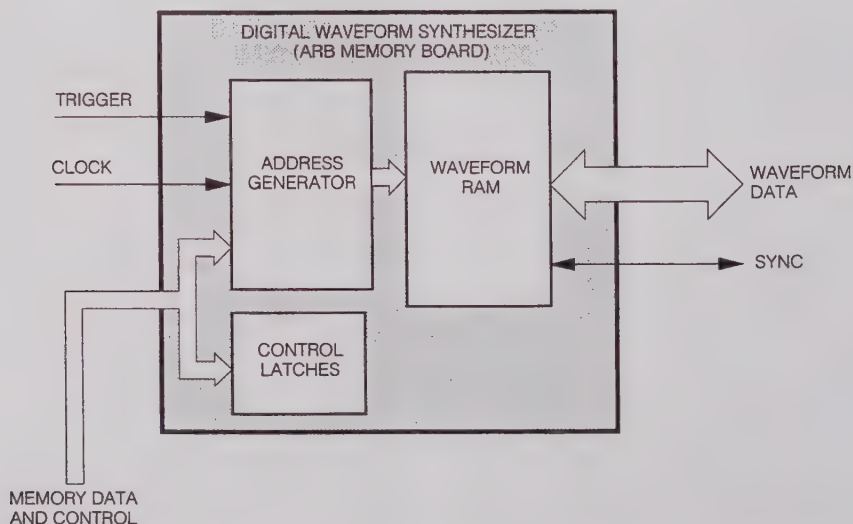


Fig. 2-3 Digital Waveform Synthesizer (Arb Memory Board)

waveform data from the Digital Waveform Synthesizer into a series of discrete, high resolution (one part in 4096) steps that closely approximate a continuous analog waveform. The magnitude of the binary waveform data and the amplitude level signal from the DAC Bus (which acts as a scale factor to control the peak output voltage) controls the amplitude of the Waveform DAC output. Conversion takes place upon the occurrence of the signal selected as the DAC Clock. The Preamp converts the current signal from the DAC to a voltage signal. If filtering is not selected, the Preamp output is sent to both the Output Amplifier/Attenuator and the Sync Buffers.

2.2.7 Filter

The Filter, composed of selectable 100KHz and 4MHz sections, can be by-passed when stepped or pulse waveforms are desirable. One or both of these filters can be selected to smooth the waveshape and attenuate unwanted harmonics. When in the Function Generator mode, the filters are automatically selected. If filtering is selected, the Filter output is sent to both the Output Amplifier/Attenuator and the Sync Buffers.

2.2.8 Output Amplifier and Attenuators

A 4-bit R-2R input attenuator network, in conjunction with the amplitude level signal to the Waveform DAC, provide a 10:1 control of amplitude into the output amplifier. The output amplifier sums the current from the 4-Bit Attenuator with the analog summing current from the Analog Interface and the current generated by the offset level signal on the DAC Bus. The amplified sum, ranging up to 20Vp-p, of these values appear as the input to the 20dB/40dB attenuator and impedance matching network. The output of the 20dB/40dB attenuators in conjunction with the 10:1 input control provide a 10,000:1 range of amplitude. The Output Amplifier and Attenuators provide the Arb Out signal as well as the sum and modulation signals to the Model 680 Mainframe.

2.2.9 Sync Buffers

The bit 12 sync signal from the Digital Waveform Synthesizer is buffered and becomes the Arb Sync on the back panel BNC. Bit 13 is combined with the positive leading edge of the waveform from the Preamp, or Filter if used, then buffered to become the Wvfm Sync on the back panel BNC.

2.2.10 Output Protection

The Output Protection opens the three output circuits, Arb Out, Arb Sync, and Wvfm Sync upon the detection

of excessive voltage on the Arb Out BNC. The Output Protection circuit does double duty by opening the outputs during the Self Test and Auto Cal functions, under software control, providing both isolation and known loads.

2.2.11 Calibration Bus Interface

The Calibration Bus from the Arbitrary Waveform Generator provides two signals to the Model 680 Mainframe for calibration and self test purposes. The interface is composed of one digital and one analog multiplexer which have inputs from several test points within the Arbitrary Waveform Generator.

2.2.12 Analog Bus Interface

The two line Analog Bus for the Arbitrary Waveform Generator has one bi-directional line. The single amplifier provides buffering for the analog summing signal in either direction depending on the state of the direction relay. A second relay provides an ON/OFF control for the summing signal between the Arb and the Model 680 Mainframe. The Amplitude Modulation source in the Output Amplifier and Attenuator has its ON/OFF control in the interface. Both the relays and the amplitude modulation ON/OFF control respond to the VME Bus control signals.

2.2.13 DAC Bus

The DAC Bus has two analog signals developed in the Model 680 Mainframe DAC, ranging from 0V to +10V, in response to the operator set points of amplitude and offset and compensation factors derived during auto cal. These signals are not buffered, but are presented directly to the summing junctions in the Waveform DAC and Output Amplifier.

2.2.14 Power Distribution Bus and Interface

The Power Distribution Bus supplies several voltages to the Arbitrary Waveform Generator from the Model 680 Mainframe. The Power Supply Interface is composed primarily of filter and bypass capacitors, however, two 12V regulators and a 5V regulator are included. The Power Distribution Bus includes the two reference voltages +10VR and -10VR (not used for power) as well as the $\pm 5V$, the $\pm 15V$ and the $\pm 24V$ power lines.

2.3 FUNCTIONAL BLOCK DIAGRAM DESCRIPTION

Refer to figure 2-4, the various detailed block diagrams that follow in this section, and the schematics in section 5. Each functional block and its relationship to others is

described. The schematic location(s) of each block is in parenthesis adjacent to the heading.

2.3.1 VME Bus Interface (1A3-1D8)

The VME Bus Interface starts with the Main Address Decoder. This circuit locates the Arbitrary Waveform Generator for the Model 680 Mainframe, regardless in which of the eight module locations it may be installed. The position identifiers, MID0-MID3 from the mainframe, advance in simple binary progression with MID0 the least significant bit. Module position one has the fixed value of 0000, while position eight has the fixed value of 0111. Address lines A20-A23 are sequenced by the mainframe microprocessor to be compared with MID0-MID3. When equality is detected, and in conjunction with A18, A19, LA16, and LA17, generate CS1-/CS3/, ONBOARD/ and ROM/. Signal LDTACK/ indicates an acknowledgement by the Arb of both a successful search by the mainframe microprocessor and successful transfer of register data to the Arb.

The VME address lines A1-A16 and eight control lines are buffered through the VME I/O Buffers which are always enabled. The VME Data Buffers are bi-directional with the direction of the 16 bits determined by a combination of control signals. Control signal ONBOARD/ must be low to select the Data Buffers and LR/W, when high, will transfer data to the Arb LD0-LD15 data bus from the VME D0-D15 data bus.

2.3.2 Local Data Latches (2A6-2A8, 2B6-2B8)

The Local Data Latches are controlled by signals developed at the VME Bus Interface. These latches provide control functions and serial clock data for the Arb. These four Octal latches are each assigned to cover a functional area of the Arb (Internal Clock Control Register, Trigger Control Register, Calibration Control Register, and Clock Select Register).

2.3.3 Arbitrary Waveform Generator Operating System ROM (1B1, 1C1)

These two ROMs contain the firmware operating system for the Arbitrary Waveform Generator. Parameters, parameter limits, VME syntax interpretation, adjustment instructions, etc. are all contained within the ROMs.

2.3.4 Trigger/Clock Input Conditioning (2A2, 2A3, 3C6-3C8, 3D6-3D8)

Refer to Fig 2-5 for the detailed block diagram for this description. The Quad Threshold DAC, U25, sets the threshold levels for both the external trigger and the ex-

ternal clock using address lines LA1 and LA2 and data lines LD0-LD7. The DAC output levels, TRLV and EXCLKLV, are summed with the -10VR reference to set a level at which the external clock and trigger must exceed in order to be recognized as a valid signal. The other two DAC outputs are not used. Refer to Table 2-2.

Table 2-2 Quad Threshold DAC Selector

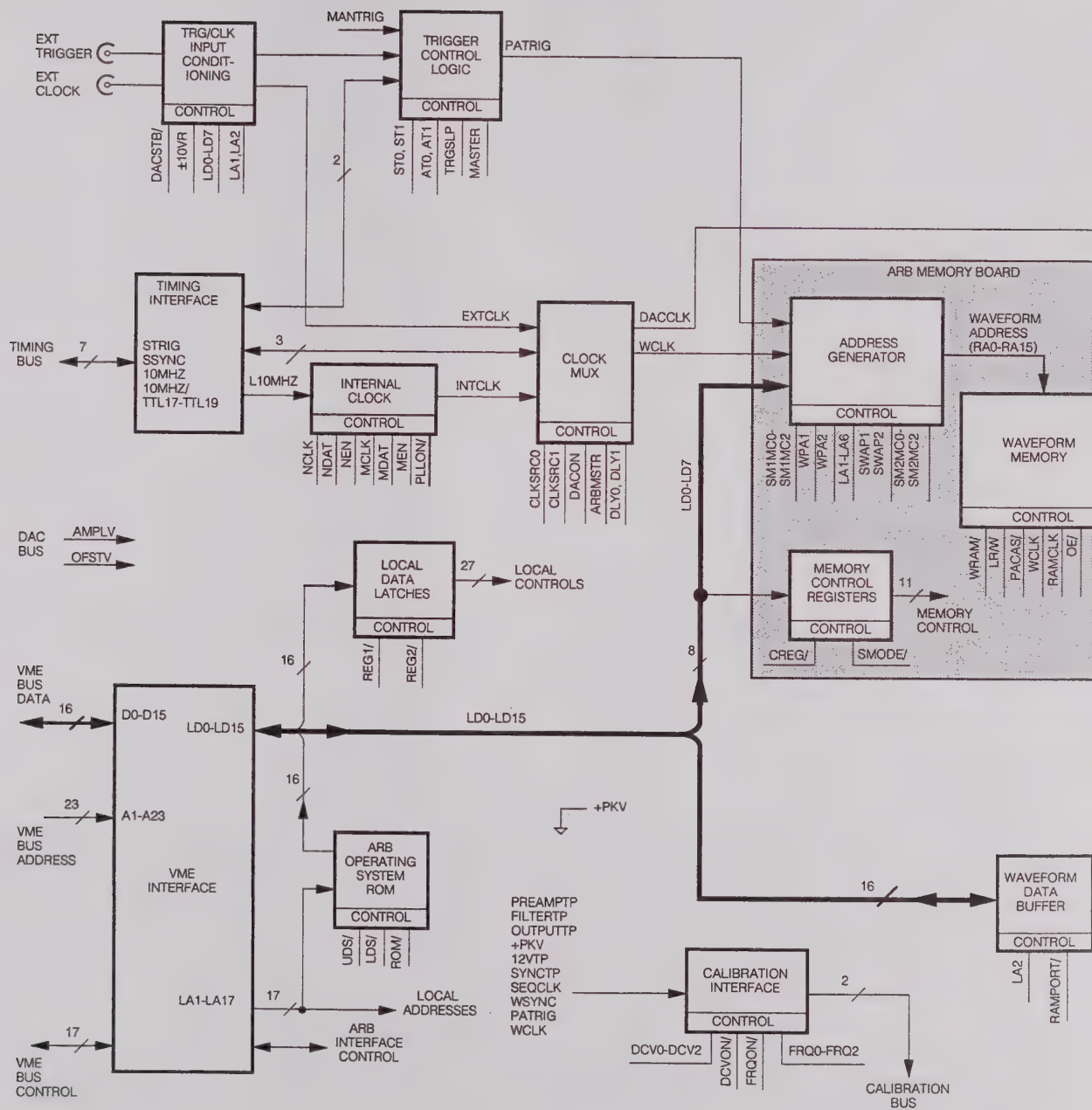
DACSTB/	ADDRESS		INPUT SELECTED
	LA1	LA2	
0↓	0	0	EXCLKLV
0↓	0	1	TRLV
0↓	1	0	SUMCALV (Not Used)
0↓	1	1	Not Used
1	X	X	NONE

2.3.5 Timing Interface (3A7, 3B7, 7D4, 7D6)

In one direction, the high speed bi-directional ECL STRIG/SSYNC lines of the Model 680 Mainframe are converted to TTL levels at the interface and become a potential source of the PATRIG signal. In the other direction, one of the TTL Arb signals WSYNC or ASYNC, selected for use by the mainframe, is applied to either the STRIG or the SSYNC lines through the TTL to ECL converters. The Model 680 Mainframe master reference signal, 10MHZ and its complement 10MHZ/, are converted from ECL to TTL levels through the differential converter at 7D4. Three bi-directional TTL clock signals (TTL17, TTL 18, and TTL19) are buffered at the interface.

2.3.6 Trigger Control Logic (3B5)

The Trigger Control Logic selects which signal (STRIG, SSYNC, the external trigger, or MANTRIG) will be used by the Arb for the waveform trigger, PATRIG, and which signal (ASYNC or WSYNC) will be applied to either STRIG or SSYNC for use by the mainframe. The external trigger slope is selected by the Trigger Control Logic. Refer to table 2-3 for the control functions.



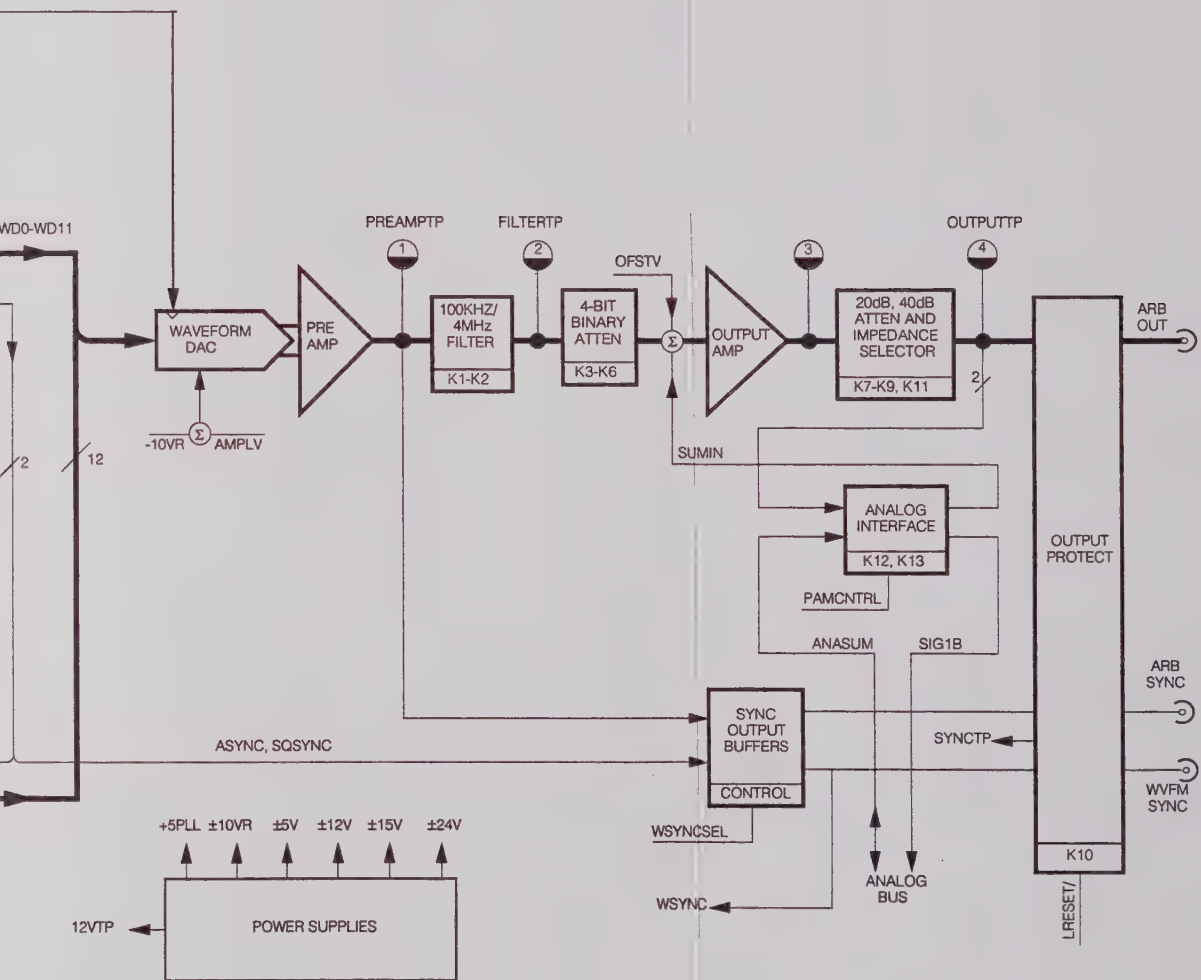


**Fig. 2-4. Model 680-01
Functional Block Diagram**

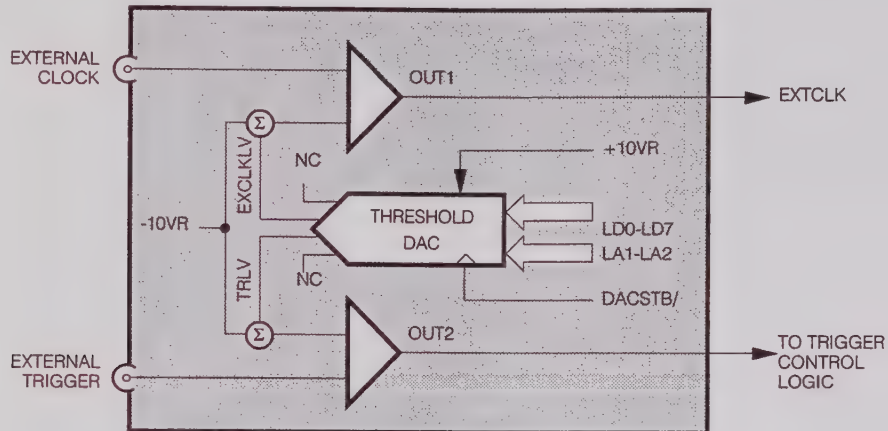


Fig. 2-5 Trigger/Clock Conditioning

Table 2-3. Trigger Control Logic I/O Selector

SIGNAL NAMES(s)	FUNCTION															
AT0, AT1	Selects the source for the Phase Accumulator Trigger, PATRIG, output. The list below shows the trigger source selections for all AT0 and AT1 combinations. <table><tr><th>AT1</th><th>AT0</th><th>Trigger Source</th></tr><tr><td>0</td><td>0</td><td>No Output*</td></tr><tr><td>0</td><td>1</td><td>System Trigger bus</td></tr><tr><td>1</td><td>0</td><td>System Sync bus</td></tr><tr><td>1</td><td>1</td><td>External Trig In</td></tr></table> *The MANTRIG input described later in the table is an exception to the "No Output" condition shown for AT0=AT1=0	AT1	AT0	Trigger Source	0	0	No Output*	0	1	System Trigger bus	1	0	System Sync bus	1	1	External Trig In
AT1	AT0	Trigger Source														
0	0	No Output*														
0	1	System Trigger bus														
1	0	System Sync bus														
1	1	External Trig In														
ST0, ST1	Selects either the ASYNC or the WSYNC signals for output on either the System Sync Bus (SSYNC) or the System Trigger Bus (STRIG). <table><tr><th>ST1</th><th>ST0</th><th>Selection</th></tr><tr><td>0</td><td>0</td><td>WSYNC to SSYNC</td></tr><tr><td>0</td><td>1</td><td>ASYNC to SSYNC</td></tr><tr><td>1</td><td>0</td><td>WSYNC to STRIG</td></tr><tr><td>1</td><td>1</td><td>ASYNC to STRIG</td></tr></table>	ST1	ST0	Selection	0	0	WSYNC to SSYNC	0	1	ASYNC to SSYNC	1	0	WSYNC to STRIG	1	1	ASYNC to STRIG
ST1	ST0	Selection														
0	0	WSYNC to SSYNC														
0	1	ASYNC to SSYNC														
1	0	WSYNC to STRIG														
1	1	ASYNC to STRIG														
TRGSLP	Selects the falling edge of the external trigger when low; selects the rising edge of the external trigger when high. Cannot select the slope of internal trigger sources.															
MANTRIG	Generates a trigger for every occurrence of this signal; this signal occurs every time the Model 680 Mainframe front panel Manual Trigger key is pressed.															

2.3.7 Internal Clock (3C2, 3D1-3D4)

The Internal clock is a Phase Locked Loop which uses the Arb L10MHZ master reference frequency as its reference input. The VCO output at U32 is set to range between 10 MHz and 20 MHz by the approximately 4V span from U29 acting upon the varactor diode in its resonant circuit. Both L10MHZ and the divided VCO output from U31 are independently divided in U30 under software control. The Phase Detect output of U30 is high if the positive edge of the divided reference frequency occurs before the positive edge of the divided VCO frequency; it is low if the positive edge of the divided reference frequency occurs after the positive edge of the divided VCO frequency; and it is in the high impedance state when the edges coincide or when non active. The Charge Amplifier integrates the Phase Detect pulses into an analog value and scales that value to span from approximately +2.5V to +6.5V. The MDAT signal into U33, under software control, divides the VCO output to yield a range between .001 Hz and 20 MHz.

The PLLON/ signal, when at a TTL high, will set the ECL to TTL converter, U53, to the high impedance state, effectively opening both the phase locked loop and the input to the final divider, U33. Refer to figure 2-6.

2.3.8 Clock Multiplexer (7D7)

The CLKSRC1 and CLKSRC0 signals select one of the four inputs: INTCLK, EXTCLK, L10MHZ, or the buffered TTL19 as the Waveform Clock, WCLK. Table 2-4 shows the combination of logic states at CLKSRC1 and CLKSRC0 that correspond to each clock selection. The ARBMSTR input signal must remain low in order to select WCLK and DACCLK. The DACON signal must be high to select a DACCLK for the Waveform DAC; the same clock source is selected for both DACCLK and WCLK. When writing waveform data to the Waveform RAM, the DAC need not be selected. The signal from the Arb placed on the TTL19 line of the Timing Bus is selected when ARBMSTR is high.

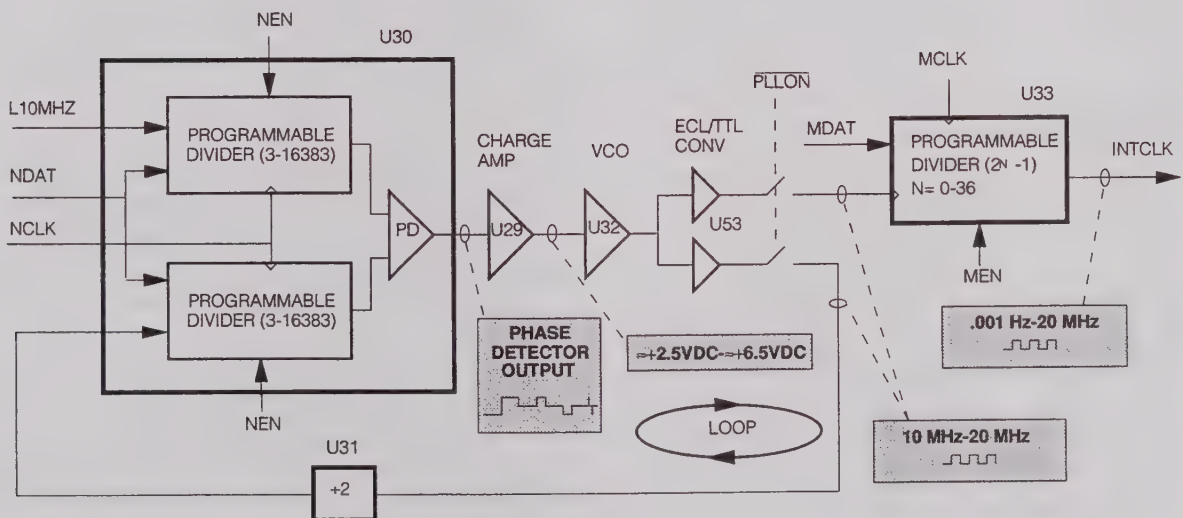


Figure 2-6. Phase Locked Loop Internal Clock

Table 2-4. Clock Multiplexer Input Selection

CLKSRC1	CLKSRC0	ARBMSTR	DACON	WCLK Selection
0	0	0	X	INTCLK (Internal Clock)
0	1	0	X	EXTCLK (External Clock)
1	0	0	X	L10MHZ (Local 10MHz Clk)
1	1	0	X	Buffered TTL19
				DACCLK Selection
0	0	0	1	INTCLK
0	1	0	1	EXTCLK
1	0	0	1	L10MHZ
1	1	0	1	Buffered TTL19
				TTL19 Selection
0	0	1	X	INTCLK
0	1	1	X	EXTCLK
1	0	1	X	L10MHZ
1	1	1	X	INTCLK

DLY0 and DLY1 are factory selected as either a low or a high permitting four values of DACCLK delay, compensating for variations in the static Waveform RAM integrated circuits. The 12-bits of waveform data must be stable at the Waveform DAC before conversion begins.

2.3.9 Digital Waveform Synthesizer (Arb Memory Board)

The Digital Waveform Synthesizer controls the retrieval of binary data from the Waveform RAM. Waveform generation takes place by sequential retrieval of digital values from the Waveform RAM on each occurrence of the Waveform Clock, WCLK, and simultaneous conversion of these data to analog voltages by a Digital-to-Analog Converter (DAC) located on the Arb Generator Board. The retrieved waveform data is 14 bits wide; bits WD0 through WD11 are converted to analog voltages by the Waveform DAC, WD12 is the ASYNC bit and WD13 is the SQSYNC bit.

A maximum of 12K locations of Waveform RAM are available for the storage of arbitrary waveform data. The entire 12K can be dedicated to one waveform or a maximum of ten waveforms may be stored. The 16K static RAM has 4K locations reserved for "standard" function generator waveforms.

Control signals that govern the operation of the synthesizer are latched from the Local Data Bus on the Arb Generator Board; address decoders in the VME Interface select the latches.

Trigger modes wait for the occurrence of the Phase Accumulator Trigger (PATRIG) before initiating the generation of a waveform period.

All of the functional blocks in the Digital Waveform Synthesizer are located on the Arb Memory Board; it shares the same enclosure with and is smaller than the Arb Generator Board. Separate schematics show the circuits for each. Refer to section 5.

2.3.9.1 Memory Address Generator (Arb Memory Board 1B4-1B7, 1D4-1D7)

The Address Generator is composed of a dual State Machine/Phase Accumulator pair. The State Machine determines the operating mode of the Phase Accumulator.

The Wavetek State Machine/Phase Accumulator Arrays accept commands and data over the Local Data and Local Address Buses. They manage the waveform synthesizing process by arbitrating read and write operations to Waveform RAM in response to front panel commands.

The Phase Accumulators operate in tandem to minimize interruptions at the output during the time that different operating modes are being selected by the user via the Model 680 Mainframe. The idle Phase Accumulator accepts new commands and data while the active Phase Accumulator continues managing retrieval of waveform data from the Waveform RAM. A change in operating mode results in the idle Phase Accumulator

taking over the tasks of waveform generation, under control of the Switch State Controller, and the active Phase Accumulator assuming the idle state ready to accept commands for yet another new operating mode.

The Burst Counter is programmable for a burst from 1 to 65,535 counts. Between a programmed frequency of 2.5 MHz and 5.0 MHz, the burst is double the entered count and for a programmed frequency greater than 5 MHz the burst count is 4 times the entered value. In the burst mode, the Burst Counter, in conjunction with the Switch State Controller, switches each Phase Accumulator as necessary to generate memory addresses. In the triggered mode, the State Machine/Phase Accumulator waits until the arrival of the trigger signal, PATRIG, to initiate address generation. Between a programmed frequency of 2.5 MHz and 5.0 MHz, two waveforms per trigger will occur and for a programmed frequency greater than 5 MHz, 4 waveforms will occur per trigger. Both the State Machine and the Phase Accumulator are Wavetek proprietary devices. Refer to figure 2-7, Arbitrary Waveform Address Generator.

2.3.9.2 Memory Control Registers (Arb Memory Board 3C4-3C7)

These registers latch the Local Data lines into the Arb Memory Board as control signals for the Address Generator and the Waveform RAM.

2.3.9.3 Waveform Memory (Arb Memory Board 2B3, 2B4, 2C3, 2C4)

The Static RAM memory is 16K or optionally 64K in size. The Waveform Data output, WD0-WD11, is presented to the Waveform DAC just prior to the delayed DACCLK signal which starts the conversion process. Both ASYNC and SQSYNC, bits WD12 and WD13, are used by the Sync Buffers to develop the sync signals. The direction of RAM waveform data (read or write) is determined by the signals LR/W and WRAM/ decoded at the VME interface. If both are low, data is written into the RAM; a read occurs when either is high.

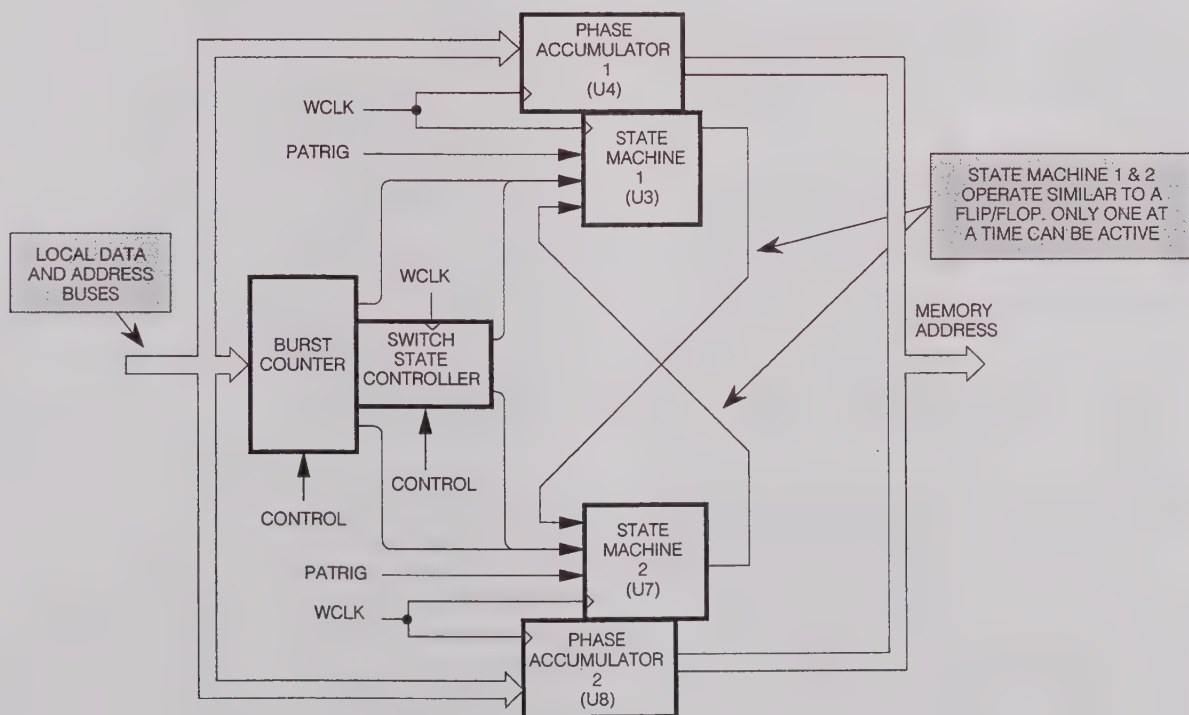


Fig. 2-7 Arbitrary Waveform Address Generator

2.3.10 Waveform Data Buffer (2A5, 2B5)

The bi-directional Waveform Buffers permit the 14 bits of waveform data to be transferred between the Arb and the Model 680 Mainframe over the VME Data Bus via the Local Data Bus. When direction control signal LA2 is low, data is transferred from the Waveform RAM to the Local Data Bus.

2.3.11 Waveform DAC (4C7, 4D7)

The high speed Waveform DAC converts the binary value represented by WD0 through WD11 into an analog voltage upon the DACCLK positive transition. The output gain of the DAC is set by the sum of the fixed voltage -10VR, from the Model 680 Mainframe, and the programmable amplitude level signal, AMPLV. The AMPLV signal is a value that is adjusted by the Model 680 Mainframe microprocessor in co-ordination with the compensation value derived at Auto Cal, operator amplitude set point, and the waveform data binary value. The differential outputs from the DAC are added together in the preamplifier.

2.3.12 Preamp (4C1-4C6, 4D1-4D6)

The Preamp is a differential amplifier composed of two transistors and a five transistor array integrated circuit. It provides the buffering function needed to drive the 4-bit attenuator and isolate the high impedance DAC output.

2.3.13 100 KHz/4 MHz Filter (4A4-4A8)

Both the low pass 3-pole 100KHz and 6-pole 4MHz filters are used to suppress most high frequency harmonics generated by the synthesizing method of waveform generation. These harmonics are related to the broadband noise components of the waveform clock, the eventual repetitive duplication of the waveform addresses in the waveform memory, any inherent non-linearity in the DAC, and aliasing. When filtering is selected, using relays K1 and K2 (refer to table 2-5), the 4MHz filter will always be in the signal path as signals of 100KHz and below are within the pass band of this filter. The 100 KHz filter provides a minimum of -45dB attenuation at an output frequency of 1 MHz and the 4 MHz filter provides a minimum of -34 dB at 16 MHz.

2.3.14 4-Bit Binary Attenuator (4A1, 4A2, 4B1, 4B2)

Combinations of K3, K4, K5, and K6 relay closures attenuate waveform current to the output amplifier. These relay contacts make closures in an R-2R resistor ladder network that permit the selection of any integer

multiple of 1 through 16 increments of current. Relay K3 has a value of 1/16, K4 a value of 1/8, K5 a value of 1/4, and K6 a value of 1/2.

2.3.15 Output Amplifier (5B3-5D8)

The Output Amplifier sums the input current from the 4-Bit Attenuator, WVFM, with the SUMIN current from the Analog Interface, and the current generated by the OFSTV from the DAC bus; and provides current gain to drive the output attenuators and load. The input stage, U45, is a high slew rate op amp forming the summing junction for the currents that determine the output level. The output from this inverting amplifier drives a current mirror input stage composed of Q3 and Q4. The following current gain stages terminate with the paralleled current sharing sets of Q9, Q11 and Q10, Q12. The combination of the variable capacitor C6 and variable resistor R201 form a peaking network and are adjusted to minimize overshoot, undershoot, and ringing using a 1 MHz square wave.

2.3.16 20dB/40dB Attenuator and Impedance selector (6D4-6D8)

The Output Attenuator system is composed of relays K7, K8, K9, and K11 and their respective resistive networks. When K9 is energized, the Arb Output is set to the no attenuation position and 50Ω output impedance. When K9 is de-energized, resistive dividers are placed into the signal path by the states of K7, K8, and K11; as a result, both the attenuation and output impedance are changed. Refer to Table 2-5, Relay Function Summary.

2.3.17 Output Protection (6B2, 6B3)

The Peak Detector circuit, part of the Output Protection, is composed of a comparator which defines an upper and lower limit of +23.5V and -23.5V for any signal on the Arb Out BNC connector. When an overvoltage occurs, the Local Data Latch controlling relays K7-K14 is set to a high impedance output. This drops the relays controlled by the latch to the normally open state causing the Output Attenuator to disengage and the output relay to open; it disables the summing features of the ANASUM bus and disconnects the Arb Sync and Wvfm Sync outputs. When output relay K10 is de-energized, the Arb Out signal is directed to the "50Ω dummy load".

The Output Protection comparator is reset with the LRESET/ signal derived from the Model 680 Mainframe signal, SYSRST/.

2.3.18 Calibration Interface (3A4, 3A5)

The Calibration Interface consists of an analog and a

Table 2-5. Relay Function Summary

Designation	Function																																																																																										
K1	Output Filters ON/OFF. Both output filters are bypassed when in the de-energized position.																																																																																										
K2	Output Filter selector. When energized, bypasses the 100KHz filter, thereby selecting the 4MHz filter. When de-energized, selects the 100KHz filter.																																																																																										
K3-K6	These relays provide an R-2R binary attenuator for coarse amplitude control as shown below. The voltages are nominal and depend on both AMPLV and the binary waveform data at the DAC. The relays with a "1" value are energized. <table><tr><th colspan="4">RELAY</th><th>OUTPUT VOLTAGE</th></tr><tr><th>K6</th><th>K5</th><th>K4</th><th>K3</th><th>0dB RANGE K7,K8/, K9/)</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1.001V</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1.626V</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>2.251V</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>2.876V</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>3.501V</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>4.126V</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4.751V</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>5.376V</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>6.001V</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>6.626V</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>7.251V</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>7.876V</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>8.501V</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>9.126V</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>9.751V</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>10.00V</td></tr></table>	RELAY				OUTPUT VOLTAGE	K6	K5	K4	K3	0dB RANGE K7,K8/, K9/)	0	0	0	0	1.001V	0	0	0	1	1.626V	0	0	1	0	2.251V	0	0	1	1	2.876V	0	1	0	0	3.501V	0	1	0	1	4.126V	0	1	1	0	4.751V	0	1	1	1	5.376V	1	0	0	0	6.001V	1	0	0	1	6.626V	1	0	1	0	7.251V	1	0	1	1	7.876V	1	1	0	0	8.501V	1	1	0	1	9.126V	1	1	1	0	9.751V	1	1	1	1	10.00V
RELAY				OUTPUT VOLTAGE																																																																																							
K6	K5	K4	K3	0dB RANGE K7,K8/, K9/)																																																																																							
0	0	0	0	1.001V																																																																																							
0	0	0	1	1.626V																																																																																							
0	0	1	0	2.251V																																																																																							
0	0	1	1	2.876V																																																																																							
0	1	0	0	3.501V																																																																																							
0	1	0	1	4.126V																																																																																							
0	1	1	0	4.751V																																																																																							
0	1	1	1	5.376V																																																																																							
1	0	0	0	6.001V																																																																																							
1	0	0	1	6.626V																																																																																							
1	0	1	0	7.251V																																																																																							
1	0	1	1	7.876V																																																																																							
1	1	0	0	8.501V																																																																																							
1	1	0	1	9.126V																																																																																							
1	1	1	0	9.751V																																																																																							
1	1	1	1	10.00V																																																																																							
K7	When energized, attenuation is selected by K8. De-energized, K7 attenuates the output from the Output Amplifier by 20 dB.																																																																																										
K8	Energizing K8 attenuates the output from K7 by 20 dB. De-energized, there is no added attenuation.																																																																																										
K9	When energized, the Output Attenuator is bypassed and there is no attenuation of the output signal; when de-energized, the output attenuation levels are selected by K7, K8, and K11.																																																																																										
K10	Energizing K10 connects the output signal to the Arb Out BNC. When de-energized, the output waveform signal is sent to an internal 50Ω "dummy" load; the Output Protection circuit remains connected to the Arb Out BNC.																																																																																										
K11	Energizing K11 selects the -40dB attenuation position of K8.																																																																																										
K12	Controls the direction of Analog Summing on the Analog Bus. When energized, the signal on the ANASUM line is summed to the Arb Out signal, via the SUMIN signal; when de-energized, the Arb Out signal is summed to the ANASUM line via the SUMOUT signal.																																																																																										
K13	When energized, connects the ANASUM line of the Analog Bus to the Arbitrary Waveform Generator.																																																																																										
K14	Directs the Sync Output Buffers either toward the output BNC connectors when energized, or the SYNCTP (Sync Test Point) when de-energized.																																																																																										

digital multiplexer which sample various points throughout the Arb, under software control, both for the Self Test and Auto Cal functions.

When the FRQON/ signal is high, the digital multiplexer goes to a high impedance (off) state. When the DCVON signal is low, the output of the analog multiplexer goes to a high impedance (off) state. Refer to Table 2-6 for input selections.

2.3.19 Analog Interface (6C7, 7B5-7B7)

The signal appearing at the Arb Out BNC can be used for Pulse Amplitude Modulating an adjacent Timing Generator by connecting to the Model 680 Mainframe SIG1B line; A logic high on the PAMCNTRL signal will make this connection. The SIG1B line on the Model 680 Mainframe connects to the adjacent higher numbered module location SIG1A line for amplitude modulating a Timing Generator.

Signals appearing on the Analog Sum line (ANASUM) can be summed to the Arb Out signal or the Arb Out signal can be summed to the ANASUM line under

control of relays K12 and K13 (refer to table 2-5). The analog Summing Amplifier converts and scales the voltage signal at its input to current. The amplifier output scale factor is 5 mA/Volt.

2.3.20 Sync Buffers (4B5, 4B6, 7C1-7C3, 7D1-7D3)

The individual waveform data bits, SQSYNC and ASYNC from the Waveform RAM, appear with each waveform data word (bits 13 and 14). The WSYNC signal is developed as the WSYNCSEL control signal gates SQSYNC through comparator U41 at the positive zero crossing of the waveform.

The SQSYNC bit is high only at the first clock period when in the Function Generator mode. When the Arbitrary Waveform mode has been selected, SQSYNC is high for the first four waveform clock periods. The ASYNC bit is high during the first waveform clock period when in the Function Generator mode and can be programmed high more than once within the period when in the Arbitrary Waveform mode.

Table 2-6. Calibration Multiplexer Input Selection

DIGITAL SECTION						
Signal Select Lines			Selected Input Signal	Signal Origin on Schematic		
FRQ0	FRQ1	FRQ2				
0	0	0	NONE			
0	0	1	SEQCLK (not used)			
0	1	0	WSYNC (Waveform Sync)			4B4
0	1	1	PATRIG (not used)			3C4
1	0	0	WCLK (Waveform Clock)			8D3
1	0	1	NONE			
1	1	0	NONE			
1	1	1	NONE			

ANALOG SECTION						
Signal Select Lines			Selected Input Voltage	Signal Origin on Schematic		
DCV0	DCV1	DCV2				
0	0	0	PREAMPTP (Preamp Test Point-TP1)			4C1
0	0	1	FILTERTP (Filter Test Point-TP2)			4B4
0	1	0	NONE			
0	1	1	OUTPUTTP (Output Test Point-TP4)			6C4
1	0	0	NONE			
1	0	1	+PKV (local signal common/ground)			5C2
1	1	0	12VTP (± 12 Volt Test Point)			7A3
1	1	1	SYNCTP (Sync Output test point)			7C1

The Arbitrary Waveform Generator module signals, ASYNC and WSYNC, are buffered then switched by relay K14 to the Arb Sync output BNC and to the Wvfm Sync output BNC respectively. The relay opens upon an overload detected by the output protection circuit or during Self Test, Auto Cal and power off. Refer to table 2-5.

2.4 AUTOMATIC DIAGNOSTICS AND CALIBRATION

Using the Model 680 Mainframe resources (DAC, DVM, frequency counter, and RAM), the Arb can be tested and adjusted. The Self Test provides a wide tolerance evaluation of the Arb circuits and indicates the result on the mainframe status display digits; while the calibration both measures and adjusts, displaying a failure on the status display. The DVM resolves its input to 12 bits while the frequency counter resolves its input to 8 bits. The DAC uses 16 bits to develop the analog adjustments which are sent to the Arb over the DAC bus.

2.4.1 Self Test

The Self Test sequentially tests the following signals in the given order: PREAMPTP, FILTERTP, 12VTP, SYNCTP, WCLK, and WSYNC. Each test is sequenced to the next test even if it fails. Eight bits (the status byte) are allocated to Self Test status and set if a failure occurs. They are displayed as two hex status digits on the Model 680 Mainframe.

By resetting the Arb and opening the output protection relay, the 4Vp-p test signal is developed across the 1% 50Ω "dummy load". The Model 680 Mainframe DVM verifies the PREAMPTP voltage lies between 1.42V and 2.14V, and sets bit "0" of the status byte if it is outside of that range. Bit "1" is set if FILTERTP fails its level test, etc. When the abort key is pressed during the Self Test, bit "7" is set and the rest of the test is discontinued. Each Hex digit represents the indicated fault in addition to any fault(s) indicated by the other digit. Refer to Table 2-7, Self Test Status Decoding and Figure 2-8, Self Test Flow Chart.

2.4.2 Auto Cal.

The Auto Cal uses the Model 680 Mainframe DVM, DAC, and Non-Volatile RAM. One positive and one negative test voltage for offset and two positive test voltages for amplitude are set and measured across the 0.1% resistor divider at OUTPUTTP: the output protect relay is de-energized engaging the 50Ω "dummy load". The deviation from nominal set point values to the actual values

required to set the two voltages are saved to memory as "m" and "b" of the equation $Y=mX+b$ and also used in calculating the ranges not tested. The amplitude is tested at the 50Ω 0dB, 75Ω 0dB, and 93Ω 0dB relay settings; the offset is tested over the same range and additionally tested at the 50Ω +6dB relay setting. Auto Cal should only be performed after the Arb and Model 680 Mainframe have reached operating temperature (A minimum of 30 minutes of uninterrupted operation with covers installed on the mainframe). The Auto Cal uses four bits for status, with only bits "0" and "1" in use; permitting a maximum displayed value of "3". Refer to Figure 2-9 for the Auto Cal flow chart.

Table 2-7. Self Test Status Decoding

DISPLAY		STATUS
MSD	LSD	
0	0	Test Pass
X	1	PREAMPTP (TP1) Fail
X	2	FILTERTP (TP2) Fail
X	3	PREAMPTP, FILTERTP Fail
X	4-7	NOT USED
X	8	12VTP Fail
X	9	12VTP, PREAMPTP Fail
X	A	12VTP, FILTERTP Fail
X	B	12VTP, FILTERTP, PREAMPTP Fail
X	C-F	NOT USED
1	X	SYNCTP Fail
2	X	WCLK Fail
3	X	SYNCTP, WCLK Fail
4	X	WSYNC Fail
5	X	WSYNC, SYNCTP Fail
6	X	WSYNC, WCLK Fail
7	X	WSYNC, WCLK, SYNCTP Fail
8	X	abort Key Pressed
9-F	X	NOT USED

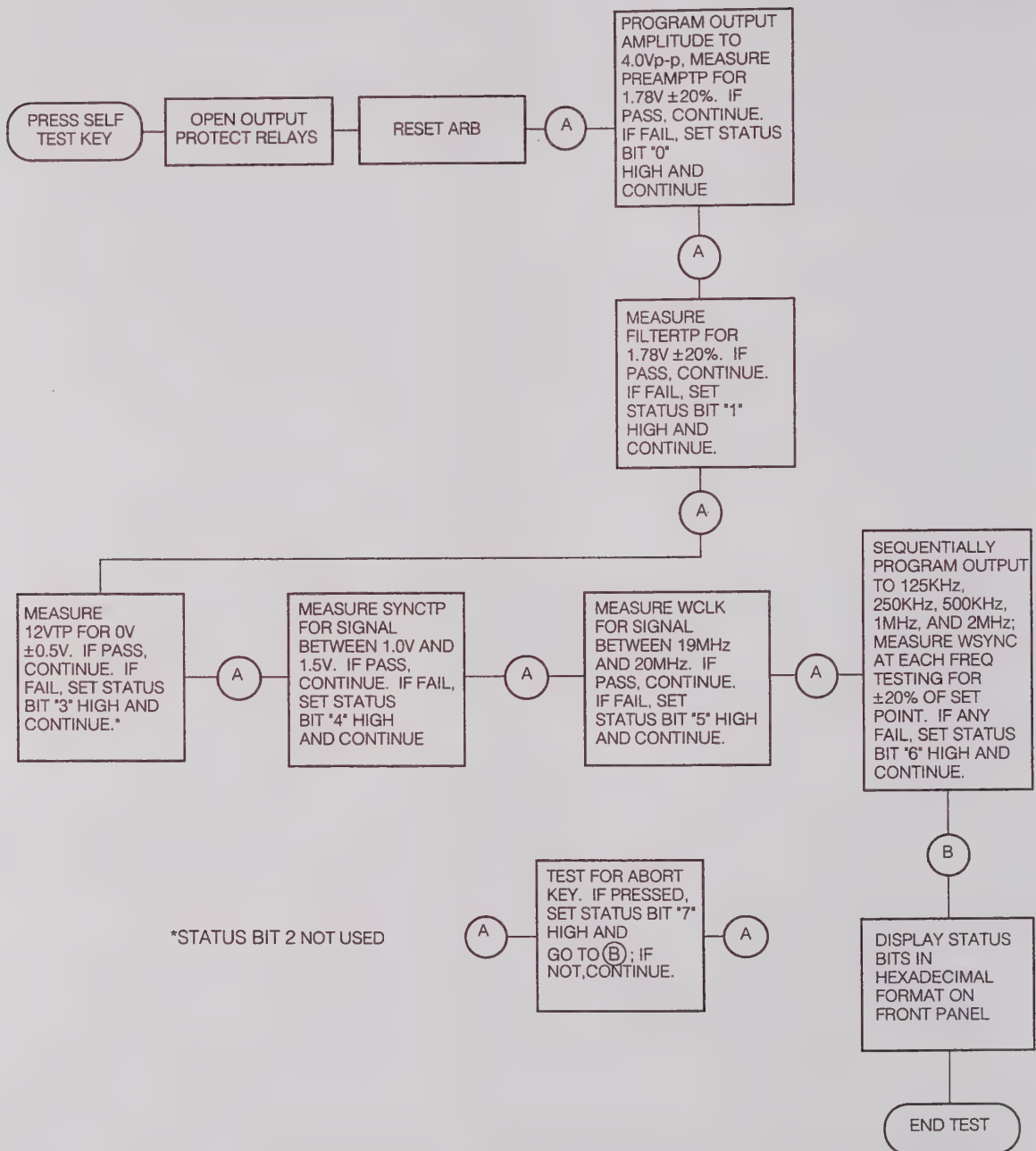


Fig. 2-8. Self Test Flow Chart.

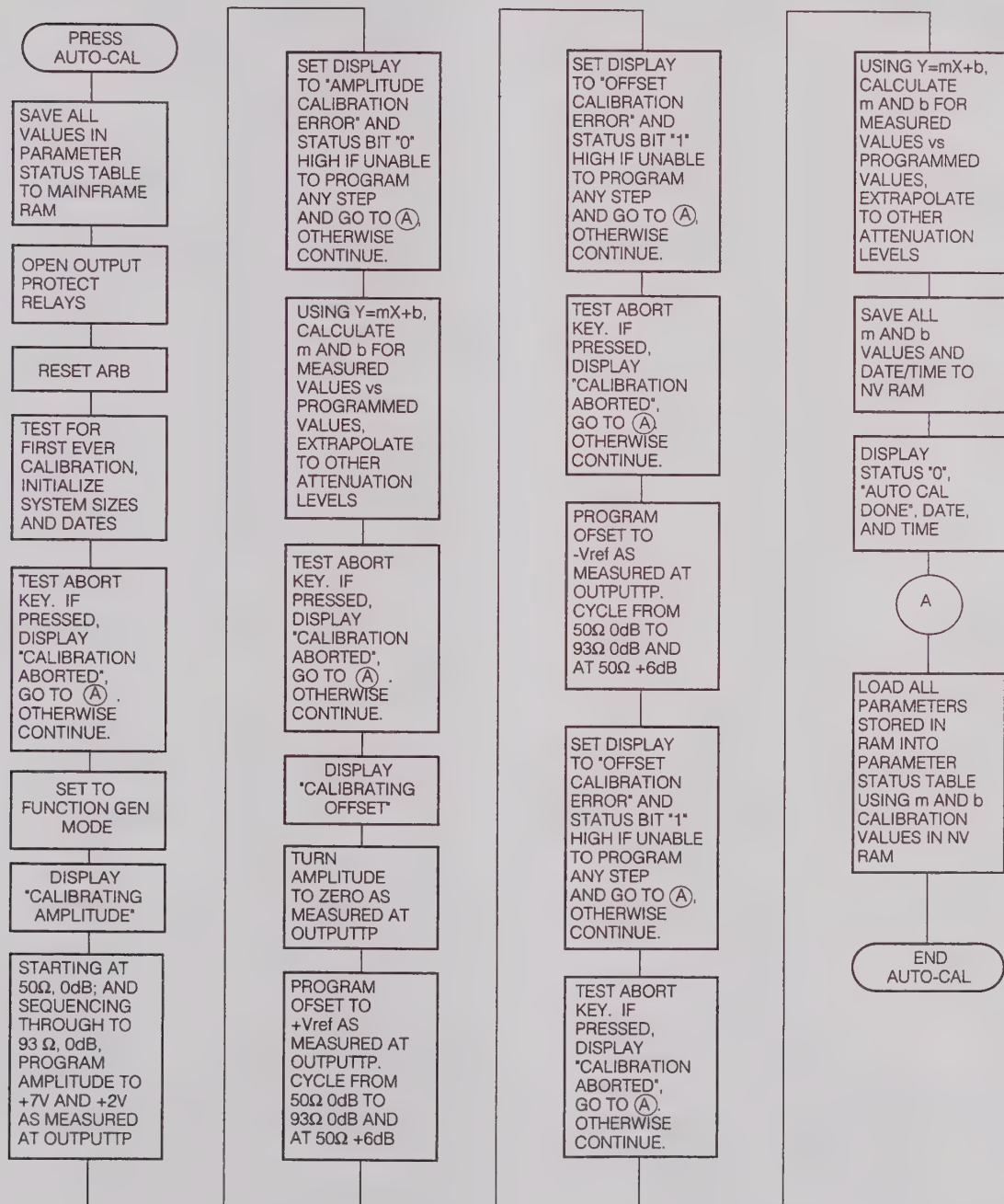


Figure 2-9. Auto Cal Flow Chart

3.1 INTRODUCTION

Table 3-1 lists the external test equipment required to manually calibrate the Arbitrary Waveform Generator. The only parameter in the Model 680 Arbitrary Waveform Generator that needs to undergo manual calibration is the aberrations/rise/fall time. It should be evaluated if the module is replaced or repaired, and adjusted if its performance is out-of-spec.

Periodic calibration of the Arbitrary Waveform Generator module is needed because of component aging, which depends upon instrument on-time and environment. Use six months as an initial manual calibration period. If possible, try to maintain accurate records of parameter values, and modify the time between calibrations based on extent of drift.

Table 3-1 Manual Calibration Test Equipment

QTY	Instrument	Suggested Model
1 3	Model 680 Extender cards	With Arb. Gen. module 96 pin extender 1100-00-3212
1	Oscilloscope	Tektronix 2465
1	50Ω load	1%, 15W

3.2 MANUAL CALIBRATION PROCEDURE

The following lists a step-by-step procedure for manually calibrating the Arb. Evaluate the signal at the Arb Out connector, J4, for the specified rise/fall time and aberration. Set the Arb frequency to 1MHz, mode to Function Generator, waveshape to square wave, and output impedance to 50Ω; use a 50Ω load. If the Arb meets the specifications, no adjustments are required. Refer to Table 3-2 for the specification. Figure 3-1 illustrates the specification.

Table 3-2 Aberration Specification

Output Amplitude	Rise time (10% to 90%)	Fall time (10% to 90%)	Aberrations
10Vp-p	≤ 25nsec	≤ 25nsec	≤ 0.5V
20Vp-p	≤ 25nsec	≤ 25nsec	≤ 2V

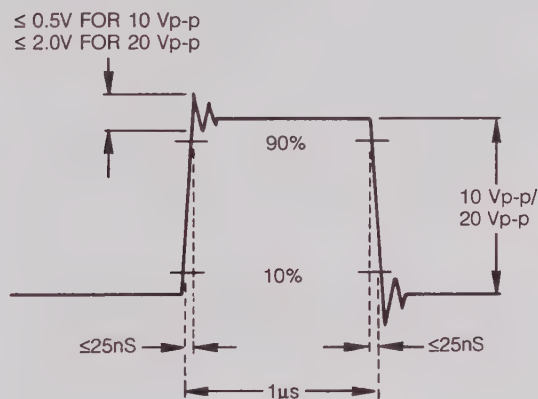


Figure 3-1 Waveform Specification

Before beginning any necessary adjustment procedure turn off the Model 680 Mainframe chassis power and then remove the Arbitrary Waveform Generator. Install the extender cards in the Arbitrary Waveform Generator module position and then plug the Arb into the extender cards, as seen in figure 3-2.

1. The first step in the manual calibration procedure is to turn on the Model 680 Mainframe power, select the Arb and set its output to:
1 MHz Square Wave
10Vp-p
50Ω load
2. Connect oscilloscope with the 50Ω load to the Arb Out BNC, J4, and adjust its controls for the best possible display consistent with measuring the specifications.
3. Adjust the variable capacitor C66 and the trimpot R201 for 500mVp-p or less of aberration (overshoot, undershoot, ringing, etc) for both the positive and negative portions of the waveform. The adjustment of each component affects the other and several iterations may be needed to meet the specifications.

4. Set the output to 20Vp-p. Verify the aberrations are $\leq 2.00\text{Vp-p}$ and the rise fall times are $\leq 25\text{nS}$. If they are not within these limits, find an adjustment position for C66 and R201 that meets the specification for both the 10Vp-p and 20Vp-p output levels.

3.3 AUTO CALIBRATION PROCEDURE

1. Turn on the Model 680 Mainframe power and select Arb. The Auto Calibration should be performed only when the Arb is temperature stabilized. A minimum of 30 minutes of uninterrupted operation with the mainframe covers installed will ensure the Arb is at a stabilized operating temperature.
2. Select "Module Cal/Test", "Autocal", and "Start". Auto calibration will be performed and the status returned. Refer to table 3-3 for calibration status.

NOTE:

"System Cal/Test" can be substituted for "Module Cal/Test". This will begin Auto Calibration of the Model 680 Mainframe and all modules installed in it.

Two adjustments can be made to the Arb by the Model 680 Mainframe Ref/Cal Board in response to the Auto Cal measurements. A compensation factor, developed in the mainframe DAC, may be added to or subtracted from the amplitude set point voltage, AMPLV, and/or the offset set point voltage, OFSTV. If the compensation adjustments are unable to bring the amplitude or offset into specification limits, a non-zero status will be returned.

Table 3-3 Calibration Status

STATUS	DEFINITION
0	Calibrated
1	Amplitude calibration failure
2	Offset calibration failure
3	Amplitude and Offset calibration failed
4-F	NOT USED

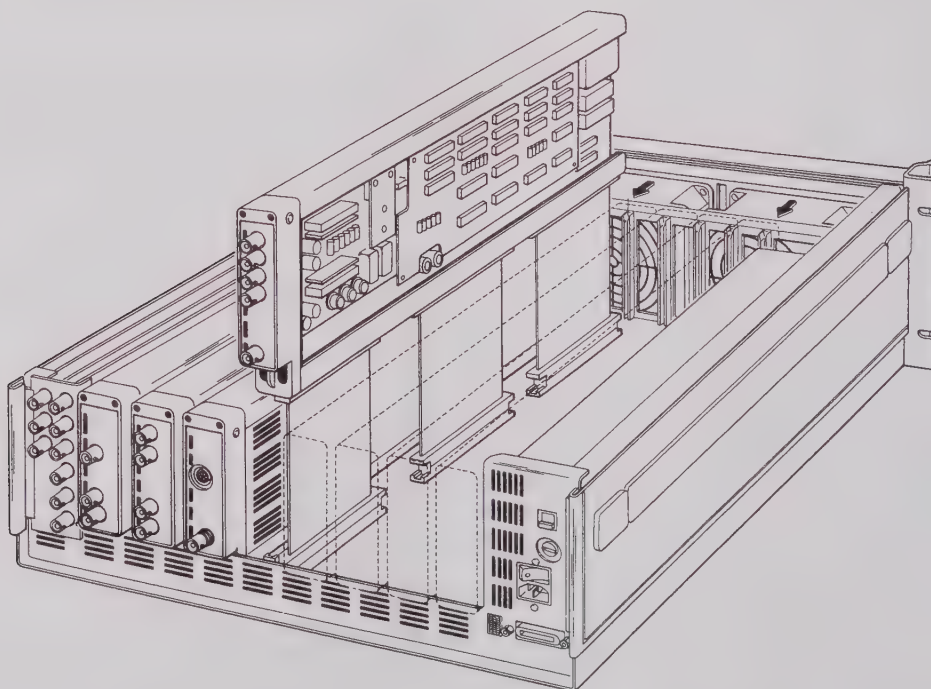


Figure 3-2. Calibration of the Arbitrary Waveform Generator

4

SECTION

TROUBLESHOOTING

4.1 INTRODUCTION

This Procedure assumes that a known working Model 680 Mainframe will be used. Verify that another Arbitrary Waveform Generator works in the unit at the module location to be used for troubleshooting. Refer to Table 4-1 for equipment required.

Table 4-1. Equipment Required

Quantity	Item
1	Model 680 Mainframe
3	96 Pin Extender Board Wavetek Part Number 1100-00-3212
1	Oscilloscope Tektronix 2465 or equivalent
N/A	Assorted hand tools

To remove the Arb Printed Circuit Board from case: Release end cap opposite BNC's, (4 screws), slide cover plate off of case, then remove 3 screws on top of case and 2 screws on back of case. Holding module with edge connectors upward, carefully slide circuit board out of case. If board does not slide freely, loosen 3 screws along the joint in the output amplifier heatsink. It may also be necessary to remove the shield in the upper right corner (2 screws) for troubleshooting.

Before beginning any of the following troubleshooting procedures, check module edge connectors for bent and missing pins. Install the three extender boards in the Arbitrary Waveform Generator module position and then plug the Arb circuit board into the extenders as shown in Figure 4-1.

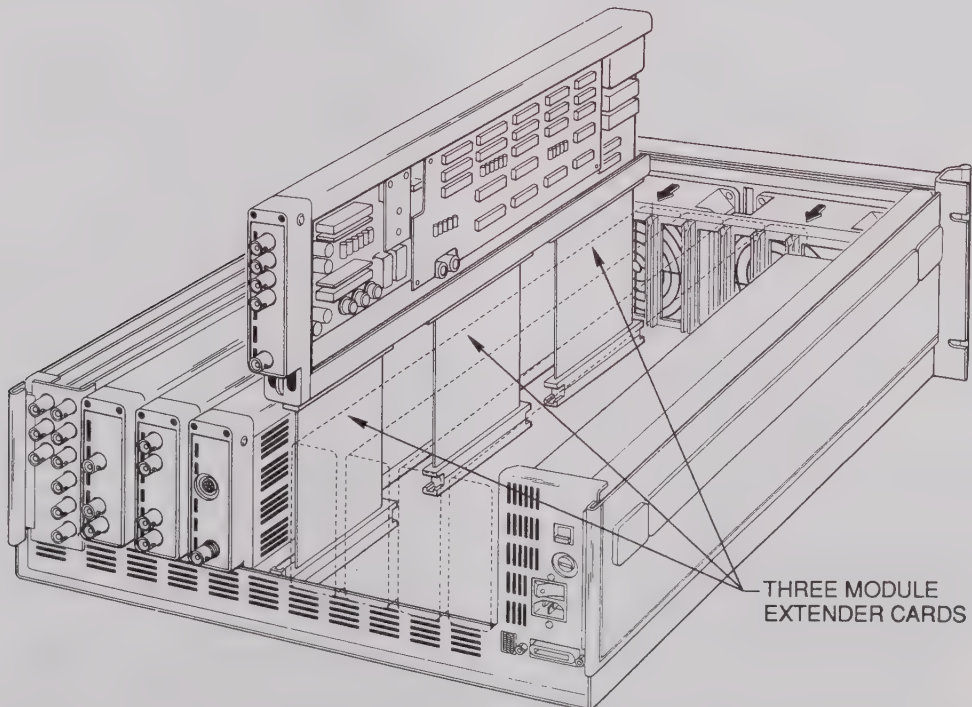


Figure 4-1. Wavetek Arbitrary Waveform Generator

Power up unit, Select module to be worked on, and Auto-Calibrate module.

Some of the Test Points referenced in the following troubleshooting procedures are under the Waveform Memory Board. With the Arb Circuit Board removed from the case, these points can be reached for test from the back of the board.

Convenient ground points for testing are the heatsink for VR1 and VR2 and a #4 screw installed in either standoff on the back of the board.

The following sections describe several Model 680-01 Arbitrary Waveform Generator failures and the step by step isolation of the problem. Turn Model 680 Mainframe power off before removing or re-installing the Arb.

4.2 NO MODULE ID

4.2.1 Symptom

When pressing the select menu, the module does not show up on the display even though it is installed in one of the eight module locations.

4.2.2 Troubleshooting Procedure

1. Check the firmware, U10 and U11 to make sure they are properly installed and none of the pins are bent or broken.
2. Isolate the problem to the VME interface circuits; either the VME bus cannot communicate with the Arb, or the Arb cannot respond to the communication.

4.3 NO OUTPUT IN CONTINUOUS MODE

4.3.1 Symptom

Pressing the following key sequence: Power **-on-**, select module number, output **-on-**, Execute: results in no output from the Arb. The desired result should be a 2 Vp-p, 1KHz sine wave at the Arb Out BNC, J4.

4.3.2 Troubleshooting Procedure

1. Verify there is a sync pulse at the Wvfm Sync BNC. Both a missing Wvfm Sync pulse and a missing output signal implies no output from the Preamp. Check TP1 for a 1KHz 3Vp-p sine wave symmetrical about ground (schematic 4B4). If TP1 has a valid signal, go to step 4.
2. The next step would be to check counter/divider, U33, pin 20 (Wavetek DNC2016, schematic 3C2) for **INTCLK**, a 20MHz TTL square wave. If this is not present, check the TTL 10MHz reference, **L10MHZ**,

at the ECL/TTL converter, U50, pin 4 or the differential ECL 10MHz input from the Model 680 Mainframe at U50 pins 2 and 3 (10H125, schematic 7D4). Verify the **L10MHZ** at the PLL, U30, pin 1 (Motorola 145157, schematic 3D4). Check the internal Phase Locked Loop clock circuit (schematic 3D3). Verify signal **PLLON** is high at the ECL/TTL converter, U53 pin 9 (10H350, schematic 3D1).

3. If step 2 is functioning correctly, check the waveform DAC, U39, pins 6 and 7 (TRW TDC1012, schematic 4C7) for 1KHz 300 mVp-p complementary sine wave. If this is not present, check the clock multiplexer, U48, pin 18 (Wavetek 8600-00-0566, schematic 7D7) for signal **WCLK** and pin 16 for signal **DACCLK**. Also check the memory board for **WCLK**, found at several locations on the board, refer to the Arb Memory Board schematic. If **WCLK** cannot be found on the memory board but is found on the main Arb board, check to see if any pins on J/P 100A are damaged. When re-installing the memory board, ensure the connectors are properly seated. After re-installing the Arb Memory Board and verifying **WCLK** on it, test the Waveform DAC pins 6 and 7 again. If the test fails, the fault lies in either the Waveform DAC or the Arb Memory Board. Replace the Arb Memory Board and test again.
4. If step 3 produced the correct results, check TP2 for a 1KHz 3Vp-p sine wave symmetrical about ground (schematic 4B4). If this step fails it could possibly indicate K1 may be faulty (schematic 4B7), or perhaps U41 (schematic 4B6) might be damaged. There also may be damage in the 4-bit binary attenuator (schematic 4B3).
5. If step 4 passed, check output test point, TP4, for 1KHz 1Vp-p sinewave symmetrical about ground (schematic 5C4). If this step fails, check the binary attenuator (schematic 4B2), the output amplifier test point TP3, (schematic 5C1) or check the relays in the output attenuator (schematic 6D4-6D8). If the incorrect relays are energized/de-energized, a failure may have occurred at the control register or drivers.
6. If the correct signal existed at TP4, and still no output exists at the Arb Out BNC, a failure may exist in K10 (schematic 6D4) or the output protection circuit is active.

4.4 NO OUTPUT IN THE TRIGGERED MODE

4.4.1 Symptom

When the 680-01 Arbitrary Waveform Generator is put into any one of several triggered modes with a known

good trigger, there is no output present at the output BNC of the Arb.

4.4.2 Troubleshooting Procedure:

Verify that the output is working in the continuous mode. If not, follow through the previous troubleshooting procedure described in section 4-3 and ensure that the Arb is functioning in the continuous mode.

To program the Arb, press the following keys: System, trig int, program frequency for 1KHz, Execute. Then select the arb module number, turn the output on, module Menu, funcgen, mode, trig, timing, freq, program frequency to 2KHz, module Menu, trig, trig in, System, Execute. At this point you should have one cycle of a 2KHz sine wave which goes off for 500 ms then repeats, alternating with the 500 ms off time.

If this output does not exist carry out the following troubleshooting procedure.

1. Check U36 pin 19 (schematic 3C5) for a 1KHz TTL square wave. If this is not present, a problem exists in the system trigger interface circuit (schematic 3B7). It could also be caused by the trigger multiplexer, U36 (Wavetek 8600-00-0467). NOTE: U36 pin 19 (**PATRIG**) should always follow the trigger input selected provided that trigger mode and trigger source input are compatible. For example, if you put the Arb in an external trigger mode and apply a trigger input to the Trigger In BNC, you would see this signal at the same repetition rate at U36 pin 19, **providing the trigger threshold level has been properly set.**
2. If the preceding step is operational, and the board worked in the continuous mode yet does not have an output in the triggered mode, it would indicate the failure exists in the Arb memory board and it is failing to trigger on the phase accumulator trigger signal. Verify the **PATRIG** signal is at each device input pin as shown on the Arb Memory Board schematic. If **PATRIG** cannot be found on the memory board but is found on the main Arb board, check to see if any pins on P/J 100A, are damaged. When re-installing the memory board, ensure the connectors are properly seated.

4.5 NO WVFM SYNC OUTPUT

4.5.1 Symptom

Power up the instrument, select the module number, turn the output on, execute. The expected output should be a 1KHz TTL square wave at the Wvfm Sync BNC, J5, and it is not present.

4.5.2 Troubleshooting Procedure

1. Verify that a 2Vp-p sinewave is at the Arb Output BNC, J4. If this is not present, follow the troubleshooting procedure for 'No Output in Continuous Mode', paragraph 4.3 and correct that failure before attempting this Wvfm Sync troubleshooting procedure.
2. If the Arb Output signal is present, check the Wavesync Generator, U41, pin 9 (NE521, schematic 4B5) for, **WSYNC**, a 1KHz TTL square wave. A failure at this point would indicate that either the **WCLK** select signal, **WSYNCSEL**, (U41, pin 5) is not a valid TTL high or U41 and its related circuitry is malfunctioning.
3. If step 2 passes, a failure has occurred in the Sync Output Buffer or K14 is open (schematic 7C2).

4.6 NO ARB SYNC OUTPUT

4.6.1 Symptom

The Arb output has been turned on, the Arb Waveform Generator mode has been selected and a waveform number and size has been selected, edit has then been selected and you have drawn some waveform but nothing is present at the Arb Sync output BNC, J6.

4.6.2 Troubleshooting Procedure

For troubleshooting, press the following key sequences: Power **-on-**, select your module, reset memory, Menu, output **-on-**, Menu, arb gen, select, wvfm# **-1-**, size **-100-**, Menu, arb gen, edit, draw, func, sine, memory, arb gen, edit, adrs **-0-**, Async, **-on-**, Menu, arb gen, edit, adrs **-1-**, async **-on-**, Menu, arb gen, edit, adrs **-2-**, async **-on-**, Menu, arb gen, edit, adrs **-3-**, async **-on-**, Menu, arb gen, edit, adrs **-4-**, async **-on-**, Execute.

After this programming, the Arb Sync output should be a 50 ms positive TTL pulse at a 1KHz repetition rate. If this is not present, check the Arb Out BNC, J4, and verify that a 1KHz sine wave exists, if not, repeat the 'No Output in Continuous Mode' troubleshooting procedure, paragraph 4.3.

1. If the 1KHz sine wave is present at the Arb Out BNC, check the junction of C88 and R176 for a 50 ms positive TTL pulse at a 1KHz repetition rate. If this signal is not present the failure may be on the memory board.
2. Verify the **ASYNC** signal is present at its source, the RAM, U15 or U17, pin 15 (Arb Memory Board schematic 2C2 and 2C3). If the signal can be seen

at U15/U17 pin 15 but not at C88/R176, there is a strong possibility of a damaged pin on the connector, P/J 100B.

3. If the signal is present at the junction of C88 and R176, but still no output exists at the Arb Sync output J6, the Sync Output Buffer is malfunctioning or K14 is open (schematic 7C2).

4.7 HOW TO DECODE A SELF TEST FAILURE

4.7.1 Programming

Turn the unit on, and then press the following sequence of keys: `Module number, Module, Cal/Test, self test, start`. At the end of Self Test, which takes approximately 30 seconds, the display should read `Test`, the date and time and it should also display a number in brackets after the words `selftest status`.

4.7.2 Status

These Self Test Hex status digits represent failures depending on whether a digit is set (failed) or reset (passed), as seen in table 4.1. For example, a Self Test status of 42 would indicate two failures; the frequency at **WSYNC** and a filter test point amplitude failure. Each Hex digit represents the indicated fault(s) in addition to any faults indicated by the other digit (X).

4.8 HOW TO DECODE AN AUTO CAL FAILURE

4.8.1 Programming

Turn the unit on and then press the following sequence of keys: `Select module, Module Cal/Test, autocal, start`. Once the Auto Cal is complete, after about 30 seconds to a minute, the display should read: `cal`, with a date, time and a status number.

Table 4-2 Self Test Status Decoding

DISPLAY		STATUS
MSD	LSD	
0	0	Test Pass
X	1	PREAMPTP (TP1) Fail
X	2	FILTERTP (TP2) Fail
X	3	PREAMPTP, FILTERTP Fail
X	4-7	NOT USED
X	8	12VTP Fail
X	9	12VTP, PREAMPTP Fail
X	A	12VTP, FILTERTP Fail
X	B	12VTP, FILTERTP, PREAMPTP Fail
X	C-F	NOT USED
1	X	SYNCTP Fail
2	X	WCLK Fail
3	X	SYNCTP, WCLK Fail
4	X	WSYNC Fail
5	X	WSYNC, SYNCTP Fail
6	X	WSYNC, WCLK Fail
7	X	WSYNC, WCLK, SYNCTP Fail
8	X	abort Key Pressed
9-F	X	NOT USED

4.8.2 Status

Only one Hex digit is used to represent the Auto Cal status as seen in table 4.2.

4.9 HOW TO DECODE A GLOBAL AUTO CAL AND SELF TEST STATUS

Three Hex digits are used to display which module or channel number had a failure when a System Self Test or Auto Cal is carried out. Each Hex digit represents the indicated fault(s) in addition to any faults indicated by the other digits (X). This is illustrated in table 4-3.

Table 4-2 Module Auto Cal Status

DISPLAY	DEFINITION
0	Auto Cal Pass
1	Amplitude failed to calibrate
2	Offset failed to calibrate
3	Amplitude and Offset failed to calibrate
4-F	NOT USED

Table 4-3 Global Auto Cal and Self Test Status

DISPLAY			DEFINITION
MSD	LSD		
0	0	0	Test/Cal Pass
X	X	1	System failure (Ref/Cal or VME board)
X	X	2	Module 1 failure
X	X	3	System and Module 1 failure
X	X	4	Module 2 failure
X	X	5	System and Module 2 failure
X	X	6	Module 1 and 2 failure
X	X	7	System, module 1 and 2 failure
X	X	8	Module 3 failure
X	X	9	System and Module 3 failure
X	X	A	Module 1 and 3 failure
X	X	B	System, Module 1 and 3 failure
X	X	C	Module 2 and 3 failure
X	X	D	System, Module 2 and 3 failure
X	X	E	Module 1, 2, and 3 failure
X	X	F	System, Module 1, 2, and 3 failure
X	1	X	Module 4 failure
X	2	X	Module 5 failure
X	3	X	Module 4 and 5 failure
X	4	X	Module 6 failure
X	5	X	Module 4 and 6 failure
X	6	X	Module 5 and 6 failure
X	7	X	Module 4, 5, and 6 failure
X	8	X	Module 7 failure
X	9	X	Module 4 and 7 failure
X	A	X	Module 5 and 7 failure
X	B	X	Module 4, 5, and 7 failure
X	C	X	Module 6 and 7 failure
X	D	X	Module 4, 6, and 7 failure
X	E	X	Module 5, 6, and 7 failure
X	F	X	Module 4, 5, 6, and 7 failure
1	X	X	Module 8 failure
2-F	X	X	NOT USED

5

SECTION

PARTS AND SCHEMATICS

5.1 DRAWINGS

The following assembly drawings (with parts lists) and schematics are in the arrangement shown below.

5.2 ERRATA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, errata pages are prepared to summarize the changes made and are inserted

inside the shipping carton with this manual. If no such pages exist, the manual is correct as printed.

5.3 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit and, if applicable, the function performed.

NOTE

An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly part number.

Drawing	Drawing Number
Arbitrary Waveform Generator	
Schematic	0004-00-0546
Assembly	0002-00-0546
Parts List	1000-00-0546
Arbitrary Waveform Generator Board	
Schematic	1104-00-3281
Assembly	1101-00-3281
Parts list	1100-00-3281
Arb Memory Board	
Schematic	0103-00-3129
Assembly	1100-00-3129
Parts list	1100-00-3129

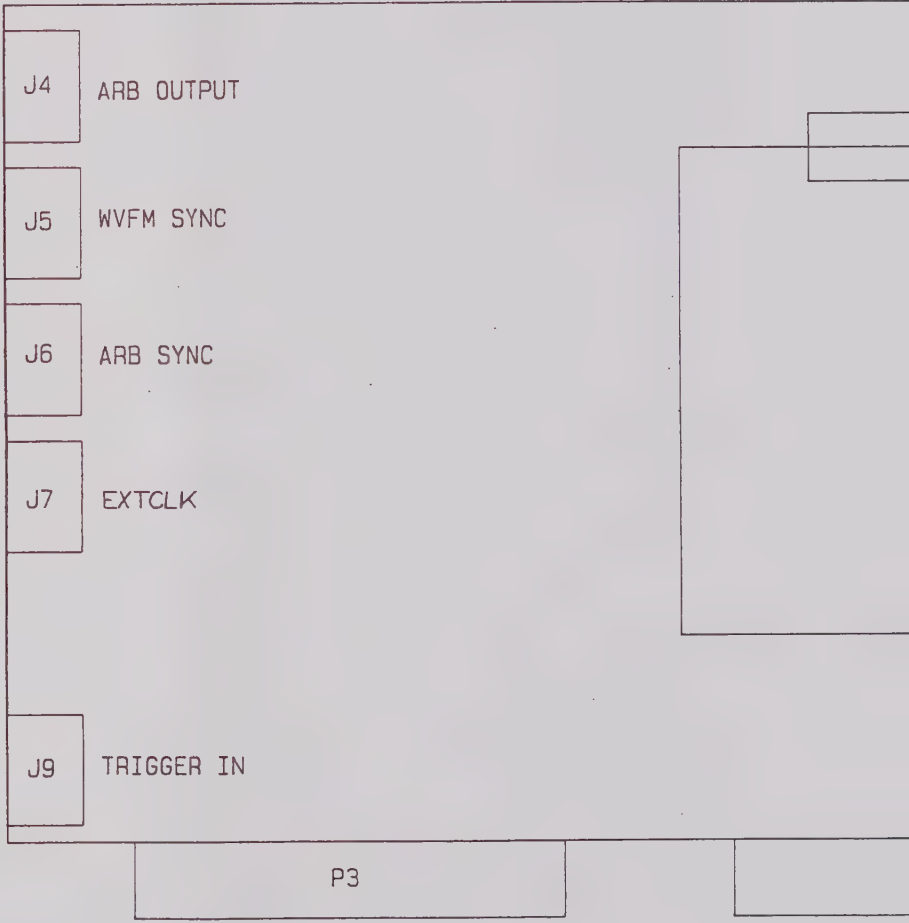
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION
AND DESIGN RIGHTS BELONGING TO HAYTEK AND MAY NOT
BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION,
OPERATION, AND MAINTENANCE WITHOUT WRITTEN AU-
THORIZATION.

D

C

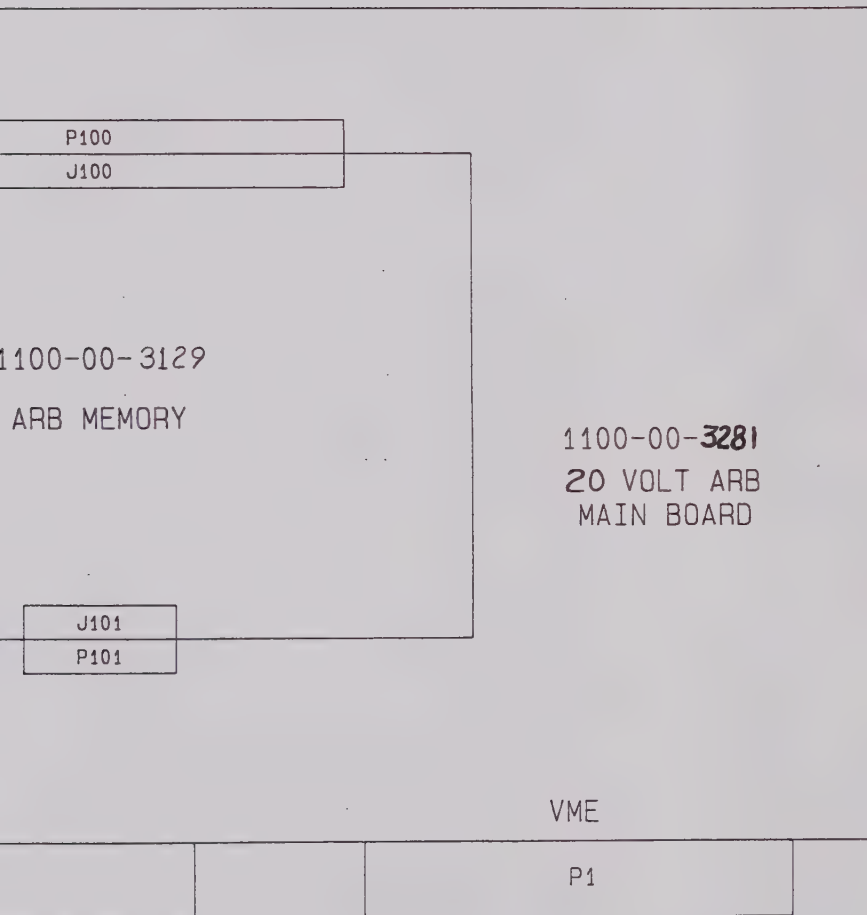
B

A



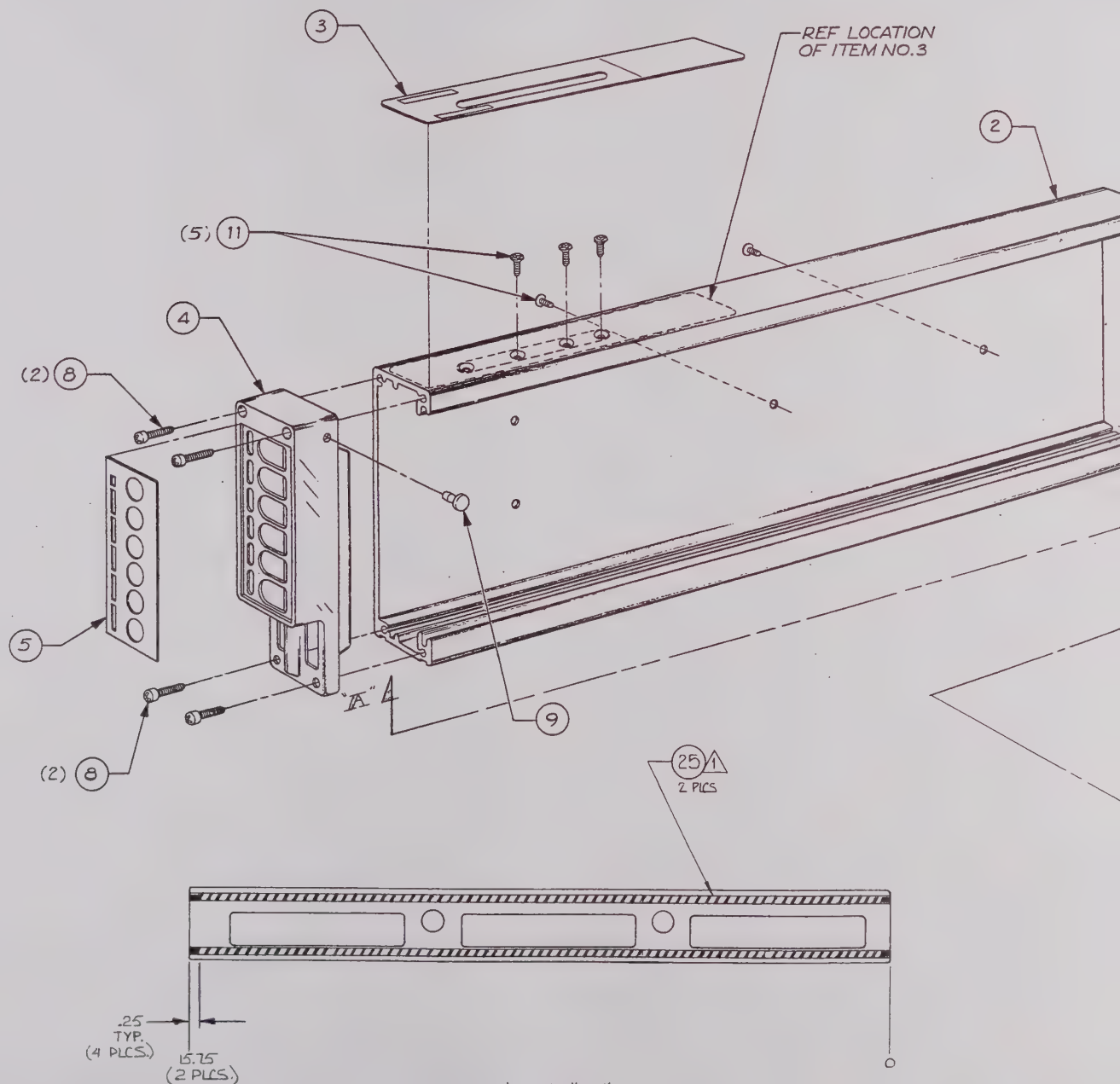
NOTE: UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP
A	ERO 9755	RO	6-7-88	CT
B	89-289	BG	5-25-89	KA



REMOVE ALL BURRS AND BREAK SHARP EDGES		DRAWN <i>RO FIFER</i>	DATE <i>5-88</i>	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL		CHECKED <i>Ed Raynes</i>	<i>6/88</i>	TITLE SCHEMATIC, INSTRUMENT 20V ARB	
FINISH WAVETEK PROCESS		PROL EMOR <i>Ed Raynes</i>	<i>6/88</i>	SIZE D 23338	
DO NOT SCALE DRAWING		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± XXX ±		DWG. NO. 0004-00-0546	
		SCALE <i>NONE</i>		MODEL <i>68001</i>	
		SHEET <i>1</i> OF <i>1</i>		REV B	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

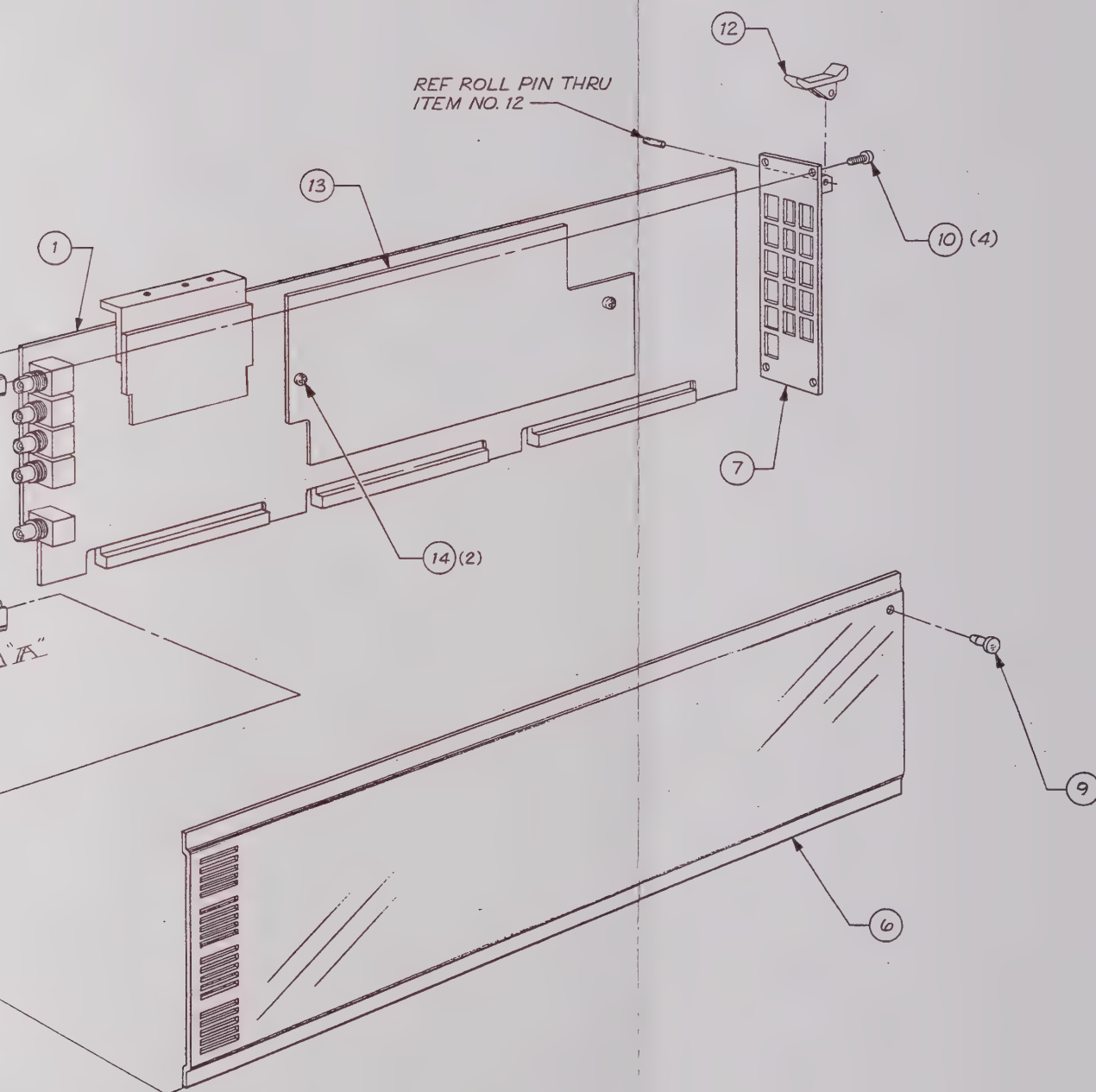


VIEW "A"- "A"

1 REMOVE ENOUGH METAL SPIRAL AT EACH END TO EXPOSE APPROX. 0.25" OF RUBBER CORE. BOND ENTIRE LENGTH OF SHIELD MATERIAL WITH CONDUCTIVE EPOXY (ITEM 26). BOND INTO GROOVE ON EACH SIDE OF HOUSING. EPOXY IS ACME 3021 OR EQUIVALENT (1600-03-0021).

NOTE: UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP
A	RELEASE ERO 9755	RO	6-7-88	ER
B	ECO # 89-057	MS	2-89	DMO



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN <i>FO FIFER</i>	DATE <i>5-28</i>	 WAVETEK SAN DIEGO • CALIFORNIA	
	MATERIAL	PROJ/EQ <i>Sol Rovers</i>		
	REL/APP'D BY <i>Don White</i>	TITLE ASSEMBLY, 20 VOLT ARB MODULE		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± 0.10 ANGLES ± 1° .XX = 0.30			
	FINISH WAVETEK PROCESS			
	DO NOT SCALE DWG	MODEL NO.	DWG NO.	REV
	SCALE NONE	680-01	0002-00-0546	B
		CODR CODE 23338	SHEET /	OF /

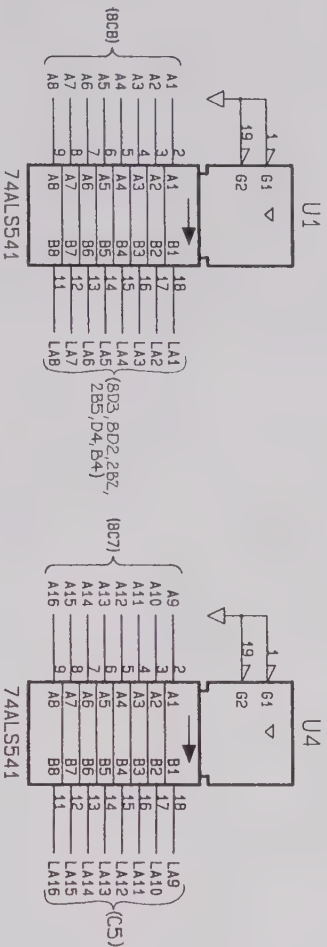
REV ECD BY DATE APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFG-PART-NO	MFG	WAVETEK NO.	QTY/PT
NONE	OUTLINE DRAWING	0002-00-0546	WVTK	0002-00-0546	1
NONE	AUTOMATIC TEST PROCEDURE	0003-00-0546	WVTK	0003-00-0546	1
NONE	INSTRUMENT SCHEMATIC	0004-00-0546	WVTK	0004-00-0546	1
NONE	PRODUCT STRUCTURE TREE	0010-00-0546	WVTK	0010-00-0546	1
13	PCA, ARB MEMORY BD	1100-00-3129	WVTK	1100-00-3129	1
1	PCA, 20MHZ ARB MEM BD-MATE I/F	1100-00-3281	WVTK	1100-00-3281	1
NONE	MANUAL, OPERATORS, 680-01 STD ARB GENERATOR	1300-00-0546	WVTK	1300-00-0546	1
7	END CAP, FORWARD	1400-02-2633	WVTK	1400-02-2633	1
5	OVERLAY, END CAP-ARB	1400-02-2690	WVTK	1400-02-2690	1
4	END CAP, REAR, MODIFIED	1400-02-2789	WVTK	1400-02-2789	1
2	HOUSING	1400-02-2903	WVTK	1400-02-2903	1
6	COVER, HOUSING	1400-02-2943	WVTK	1400-02-2943	1
3	LABEL-MODULE ID & S/N	1400-02-3130	WVTK	1400-02-3130	1
NONE	SHIM	1400-02-4977	WVTK	1400-02-4977	4
NONE	ADHESIVE	85	HENKEL	1600-03-0014	1
TITLE MODEL 680-01 ARB		ASSEMBLY NO. 1000-00-0546			REV C
WAVETEK PARTS LIST		PAGE 1			

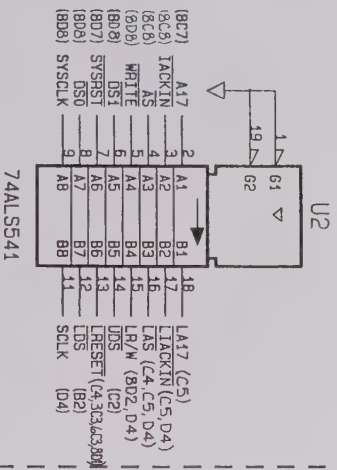
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFOR-PART-NO	MFOR	WAVETEK NO.	QTY/PT
	(CYANOACRYLATE)				
NONE	ADHESIVE, INSTANT GEL	#5440	LXTIT	1600-03-0022	1
12	PC BD EJECTOR	103 WHITE	CALPK	2800-07-0008	1
9	FASTENER, SPLIT STEM, DOWEL HD	138-NN-5426	PLACO	2800-09-0044	2
10	SCREW, 4X1/4 PHP BMS TYPE B RECESS, 4-40X1/4	4-24 X 1/4	CHRCCL	2800-22-4142	4
11	SCREW, 4-40X5/16, FHP, 1 00 DEG. Z	4-40 X 5/16	CHRCCL	2800-23-4105	14
14	SCREW, 6-32X5/16 PHP, NYLON PATCH, Z PATCH, 6-32 X 5/16	6-32X 5/16 NYLON	CHRCCL	2800-23-6105	4
NONE	PLUG BUTTON	2643/DP-500 BLACK	HEYCO	2800-35-0003	1
8	SCREW, FIL HD, PLPS, 4-24X1/2	4-24X1/2	CHRCCL	2800-39-4208	4
NONE	SCREW, 6-32X3/8 FH 100 PHLP, Z 6-32 X 3/8	6-32 X 3/8 F. H. 100	CHRCCL	2800-44-6106	1
NONE	GASKET, EMI/RFI, ELASTO MER CORE	2020-2040-0171	TECH	3000-00-0185	2.5
TITLE MODEL 680-01 ARB		ASSEMBLY NO. 1000-00-0546			REV D
WAVETEK PARTS LIST		PAGE 2			

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA			
MATERIAL	CHECKED		TITLE PARTS LIST 680-01 ARB			
	PROJ. ENGR.					
	RELEASE APPROV.					
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:		SIZE	PSCM NO.	DWG. NO.	REV
	FRACTIONS DECIMALS ANGLES XX ± XXX ±		D	23338	1000-00-0546	G
DO NOT SCALE DRAWING			SCALE	MODEL 680-01	SHEET 1	OF 1

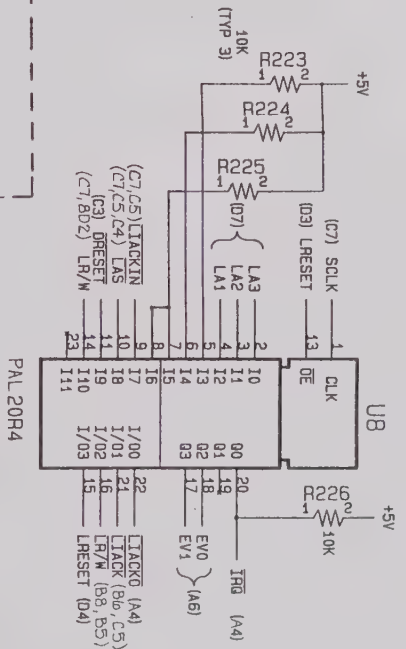
REV	ECO	BY	DATE	APP
A	ECO #89-483	MS	7/1/89	MM
B	ECO #89-584	MS	7/1/89	MM
C	ECO #89-697	MS	7/1/89	MM
D	ECO #89-798	MS	7/1/89	MM



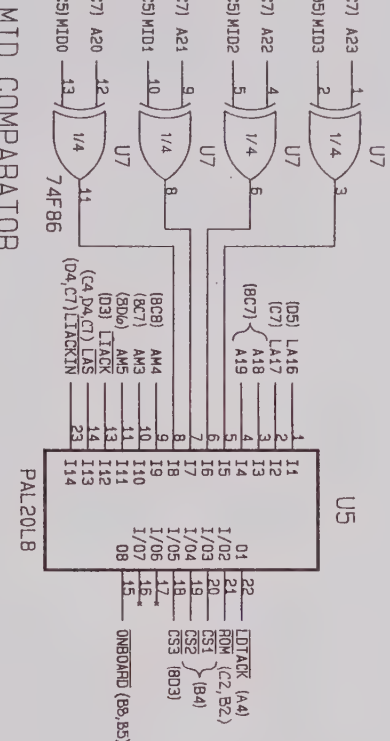
VME I/O BUFFERS



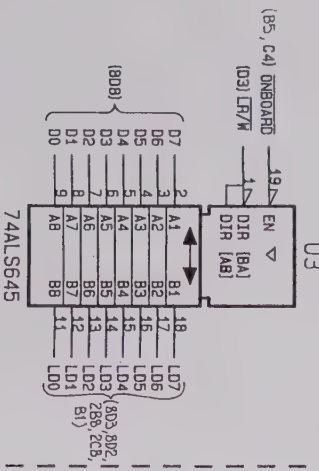
MAIN ADDRESS DECODER



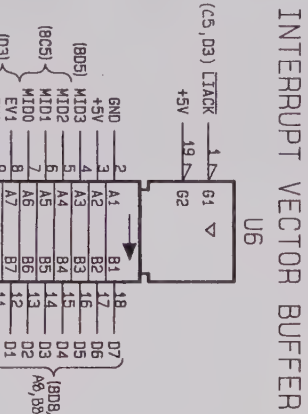
INTERRUPT CONTROLLER



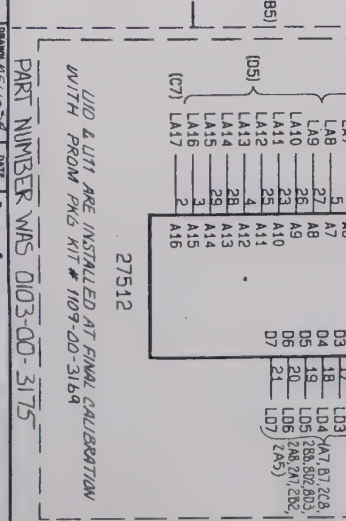
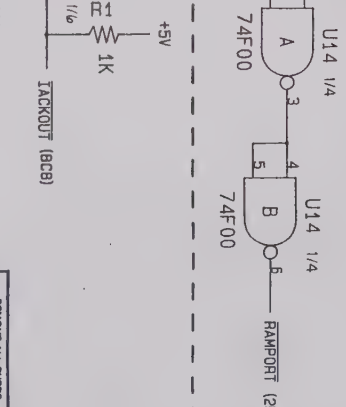
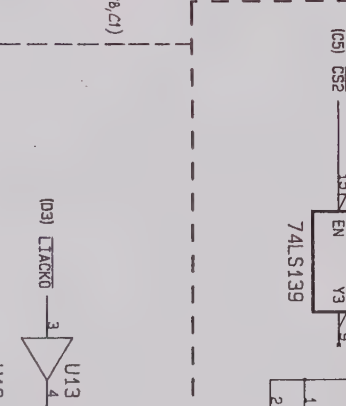
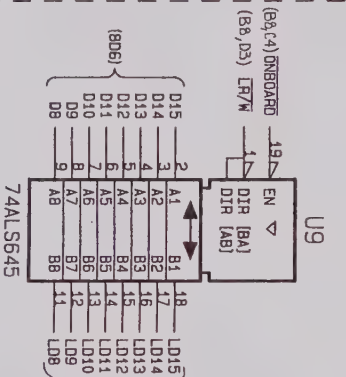
MID COMPARATOR



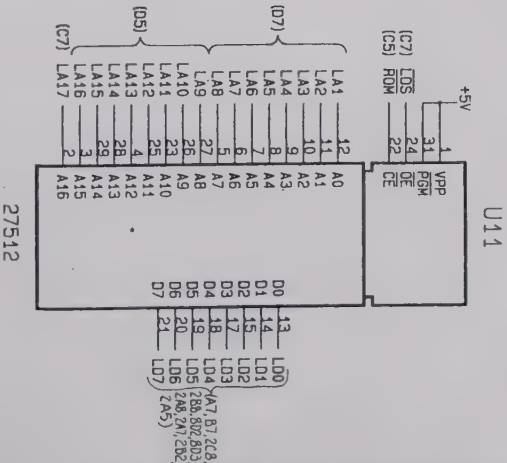
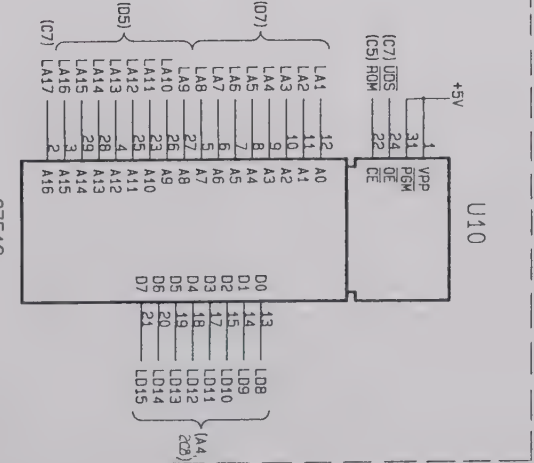
DATA BUFFERS



INTERRUPT VECTOR BUFFER



MODULE FIRMWARE



U10 & U11 ARE INSTALLED AT FINAL CALIBRATION
WITH PROM PKG KIT # 1109-00-3164

PART NUMBER WAS 0103-00-3175

WAVEFORM

SCHEMATIC

ARB GENERATOR

23338

1104-00-3281

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

DATE 7/1/89

BY 7/1/89

CHKD 7/1/89

APP 7/1/89

REV D

SCALE 1 OF 2

DO NOT SCALE DRAWING

REMOVE ALL BURNS
AND BREAK SHARP EDGES

FINISH
WAVEFORM PROCESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
FRACTIONS 1/16

SIZE 1/16

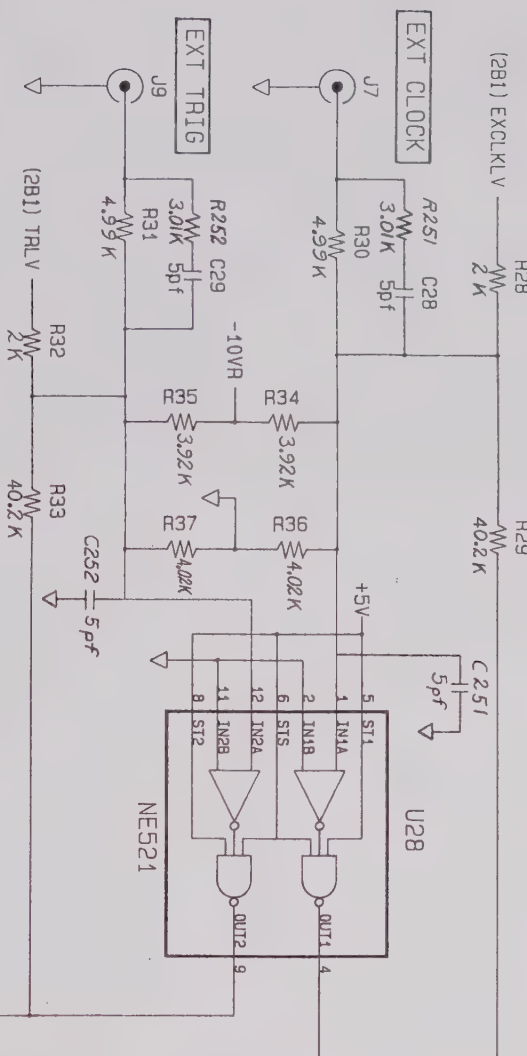
DATE 7/1/89

BY 7/1/89

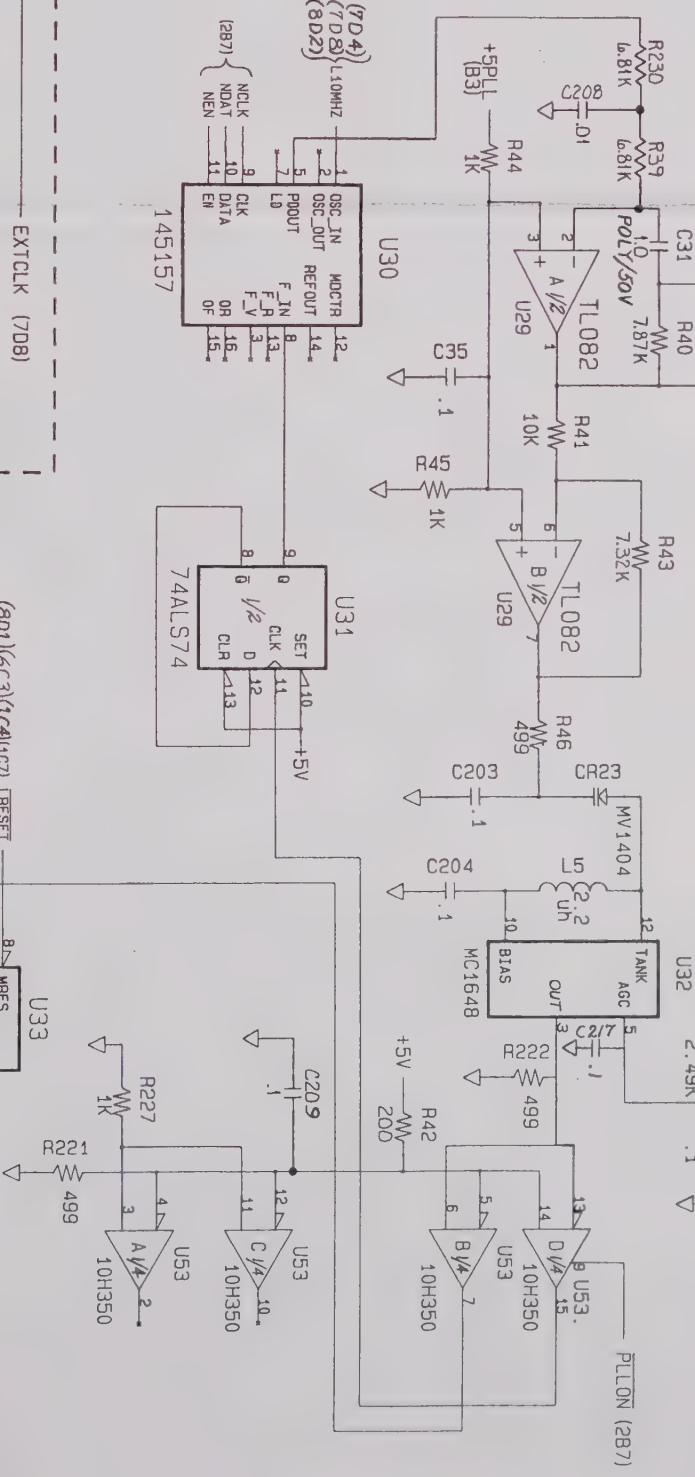
CHKD 7/1/89



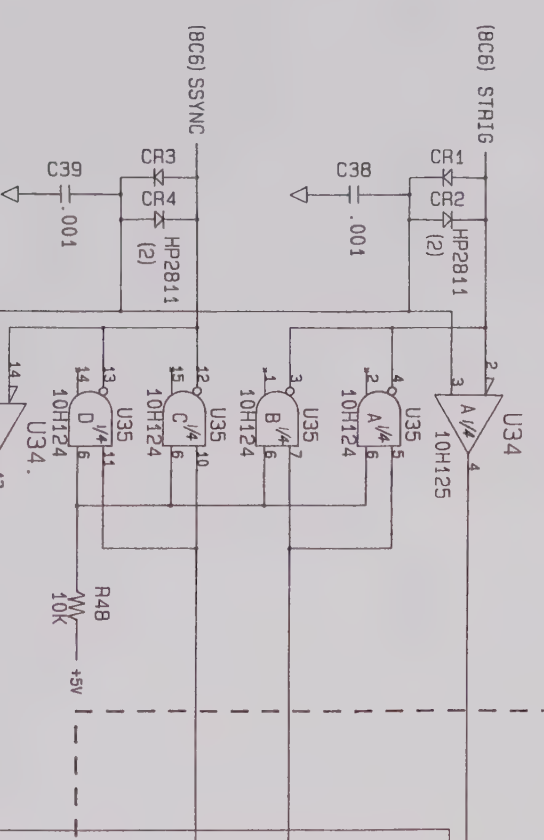
TRIG/CLOCK INPUT CONDITIONING



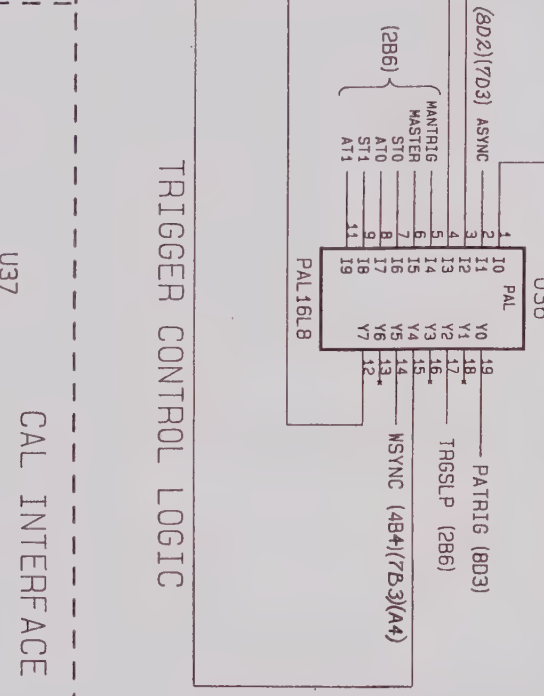
INTERNAL CLOCK SOURCE



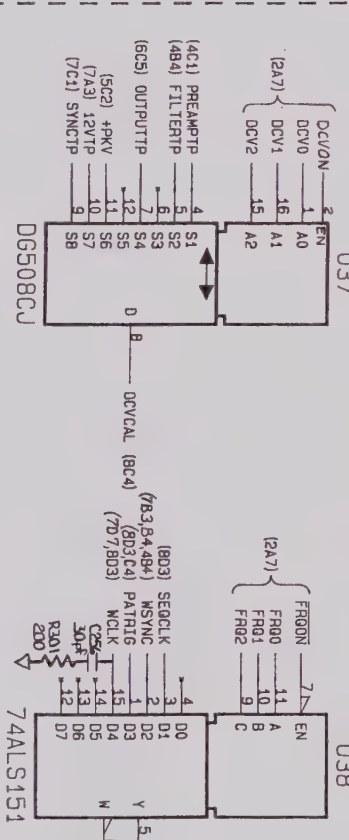
SSYNC\STRIG INTERFACE



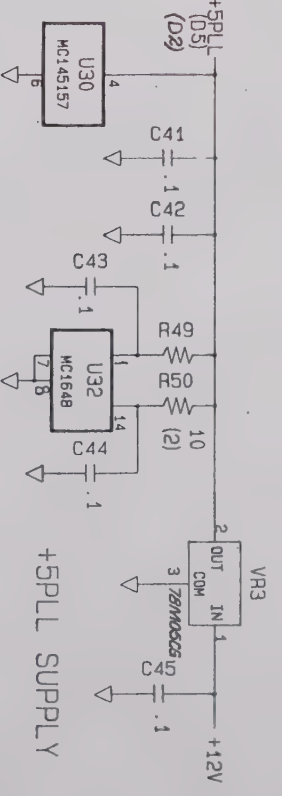
TRIGGER CONTROL LOGIC



CAL INTERFACE



+5VLL SUPPLY



SCHEMATIC

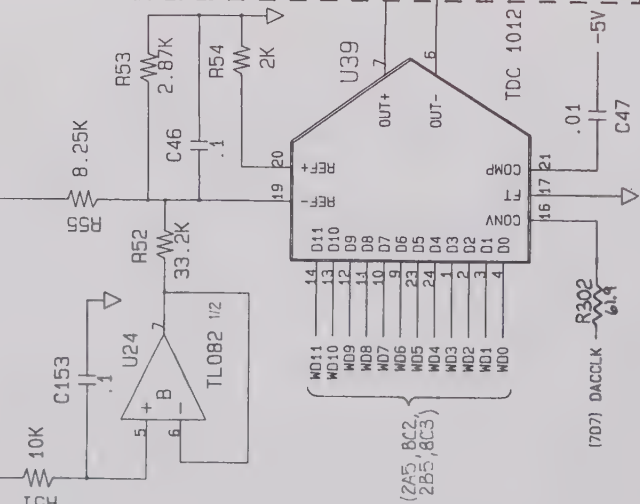
WAVETEK	DATE: 11/04/87
ARF GENERATOR	SCALE: 100%
23338	1104-00-3281
D	D

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON, EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

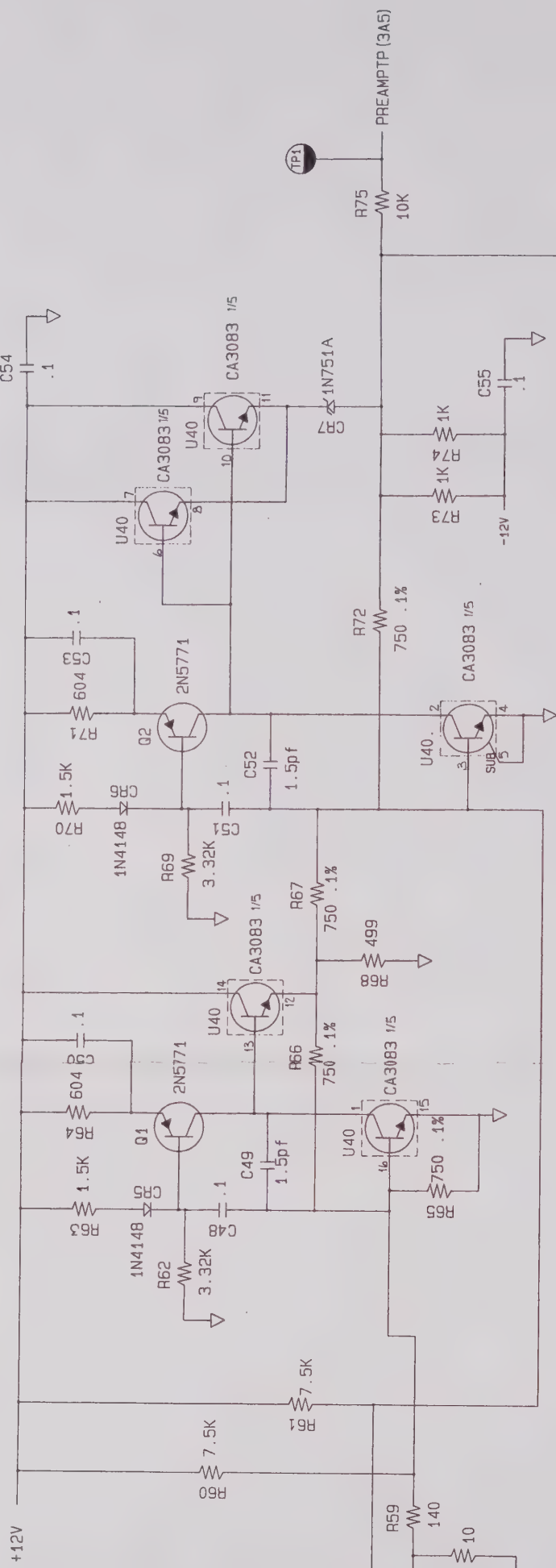
WAVEFORM DAC

AMPL V ($\pm 2.5V$)
(BC4)

(8C4)
-10VR



PRE AMP

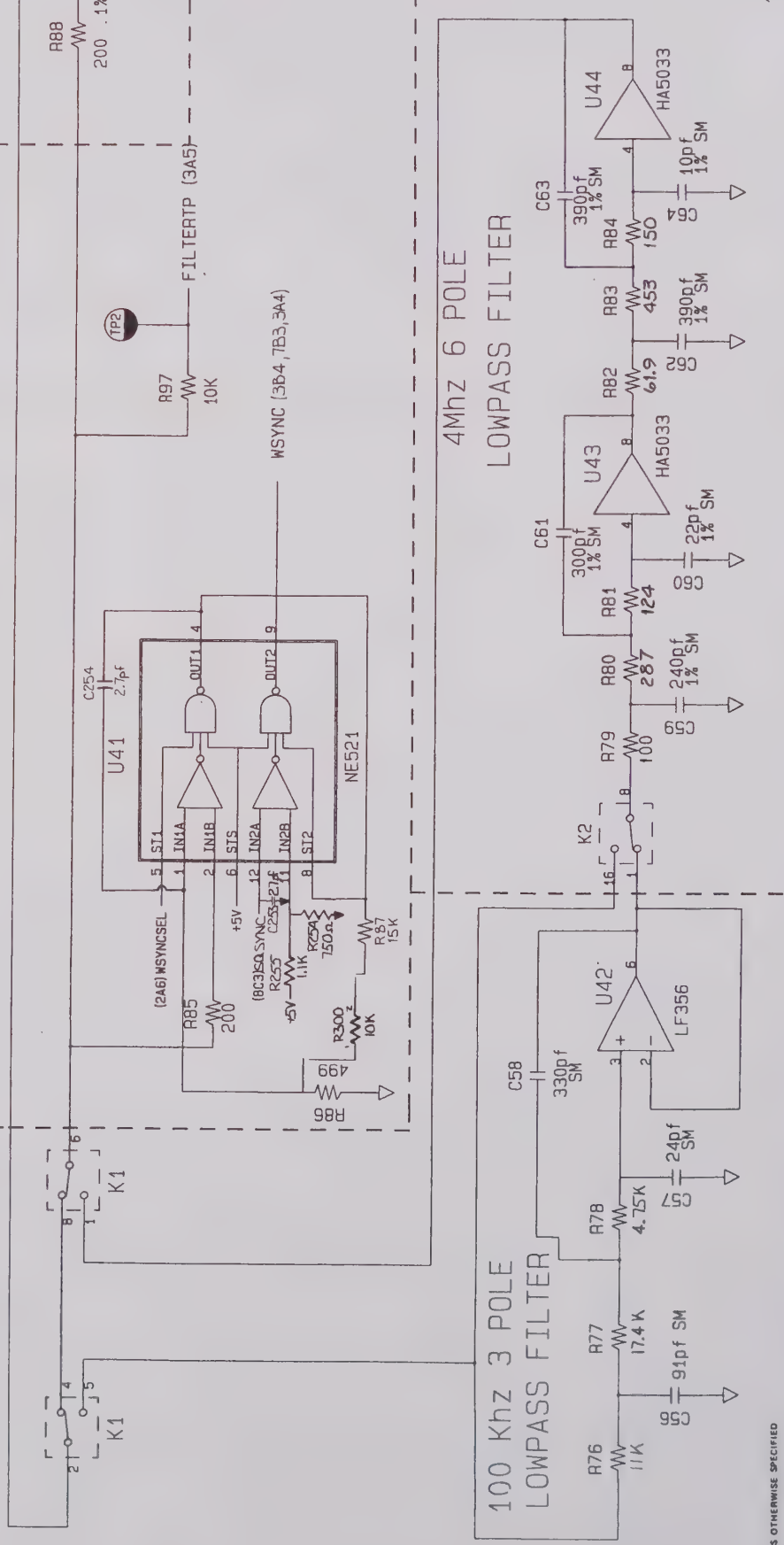


D

C

B

A



4 BIT BINARY ATTENUATOR

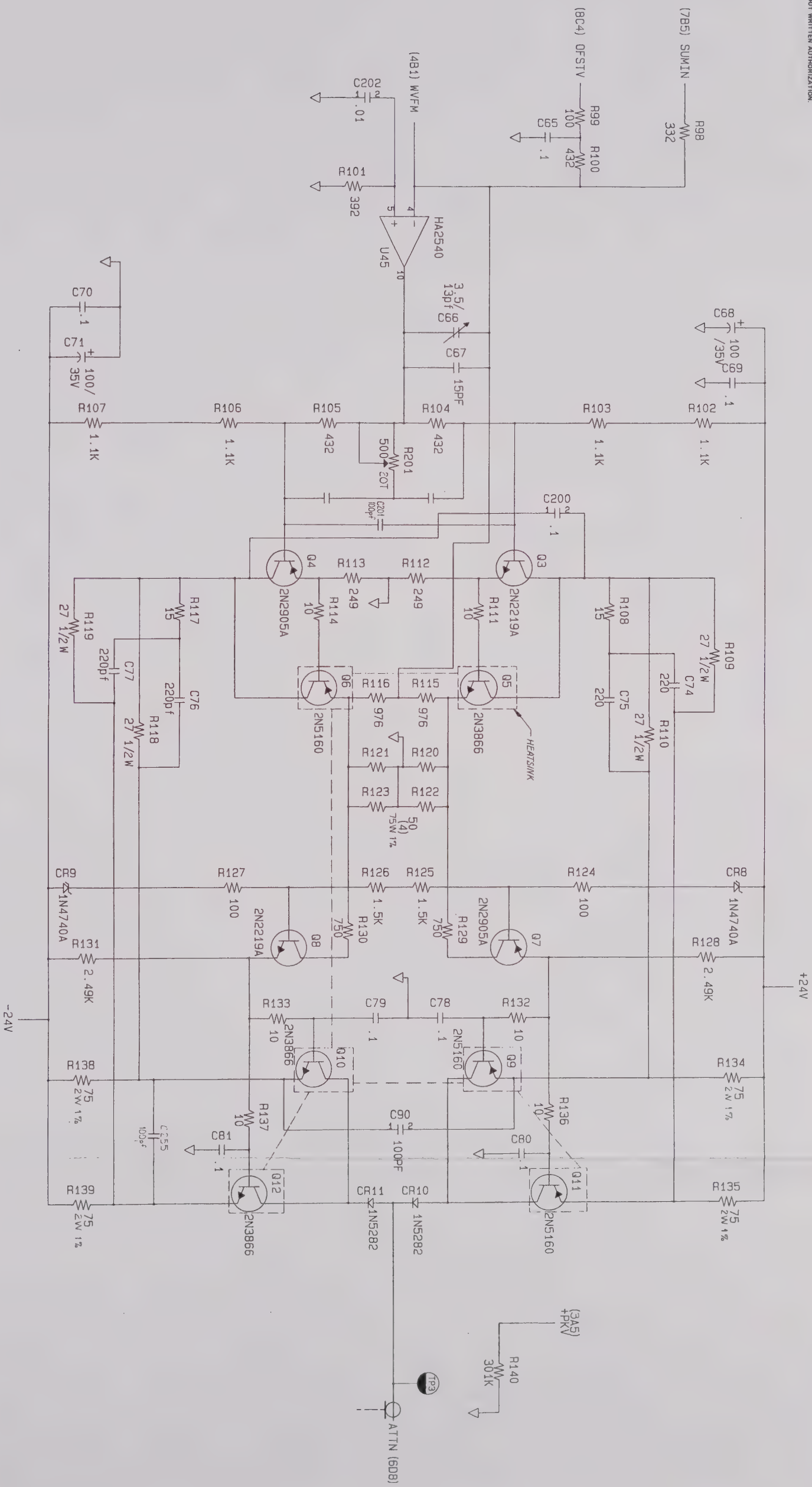
4Mhz 6 POLE LOWPASS FILTER

100 KHz 3 POLE LOWPASS FILTER

REV	ECN	BY	DATE	APP
1	1			
2				
3				
4				
5				
6				
7				
8				

REMOVE ALL BURRS AND BREAK SHARP EDGES	DATE 1/14/79	TITLE SCHEMATIC ARB GENERATOR
MATERIAL	PROJ NO 23338	SCALE DO NOT SCALE DWG
FINISH WAVETEK PROCESS	RELEASE APPROV XXX : 010 XX : 030	MODEL NO 880-001
		REV 1/04-00-3281
		SHEET 4 OF 8

NOTE: UNLESS OTHERWISE SPECIFIED



OUTPUT AMPLIFIER

WAVEJET
SAN DIEGO - CALIFORNIA

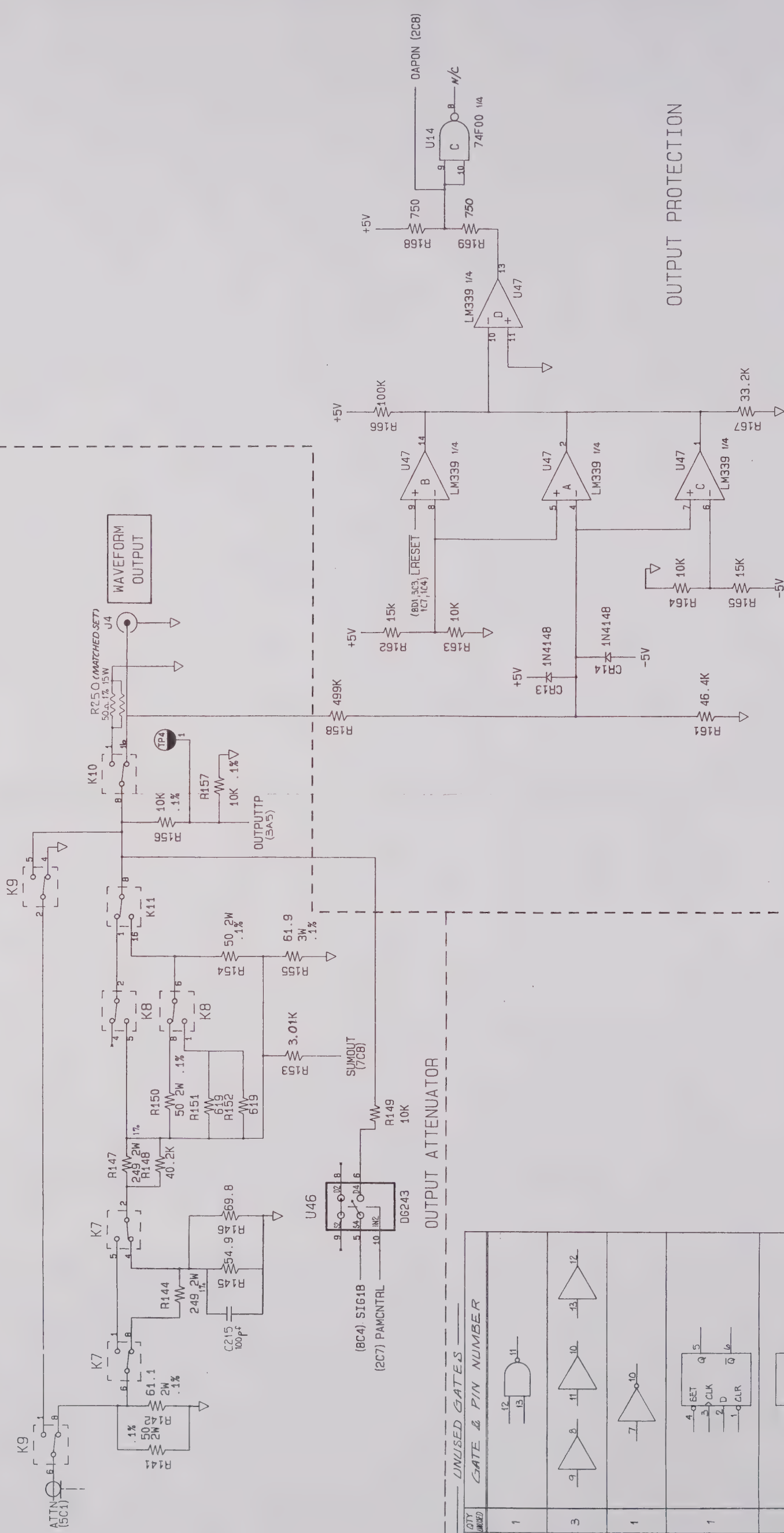
SCHEMATIC
ARB GENERATOR

MODEL NO. 880-001
DATE 1104-00-3281

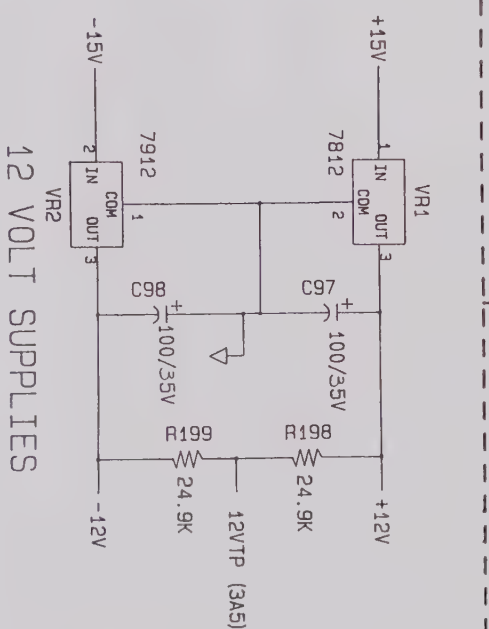
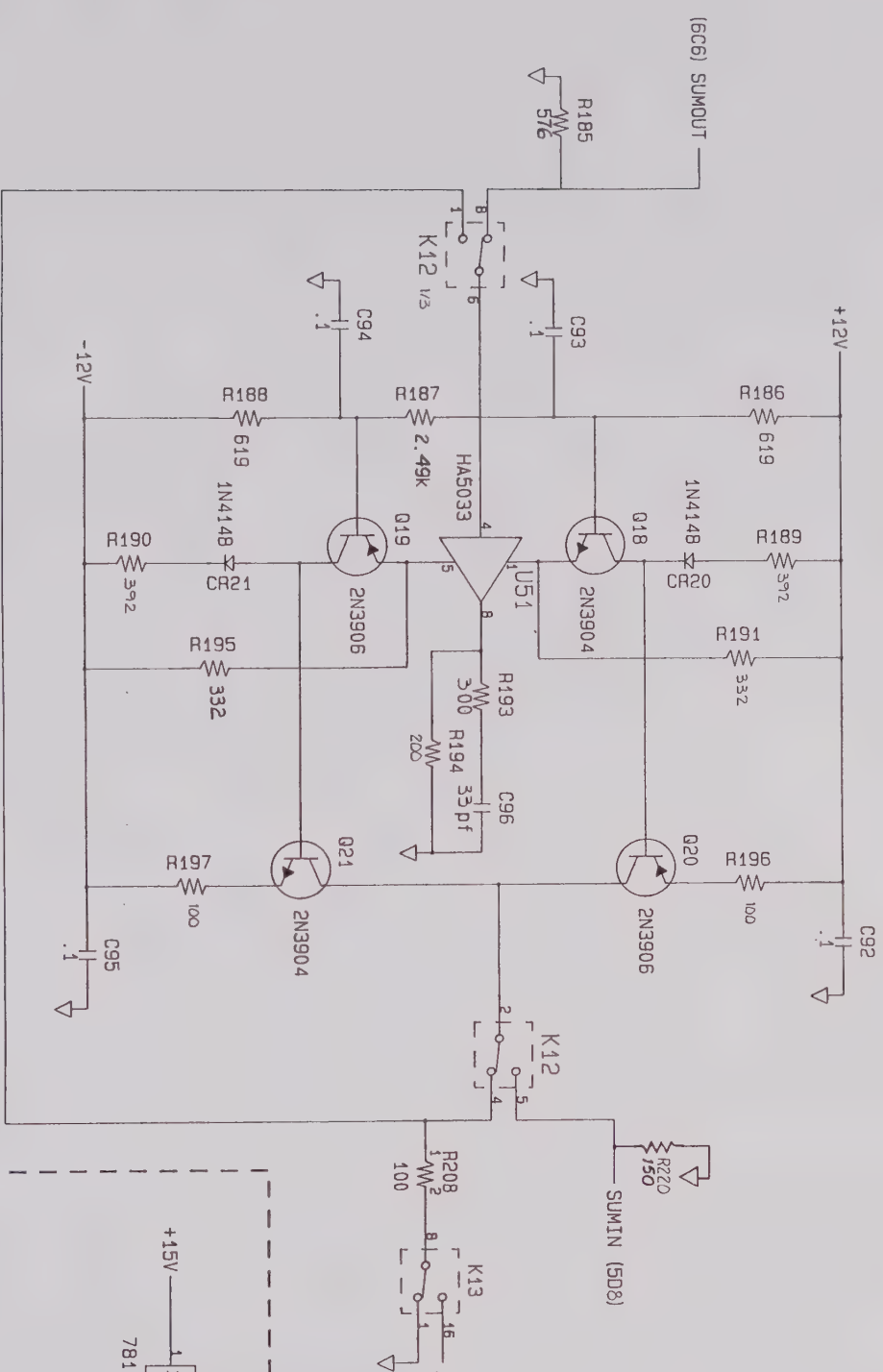
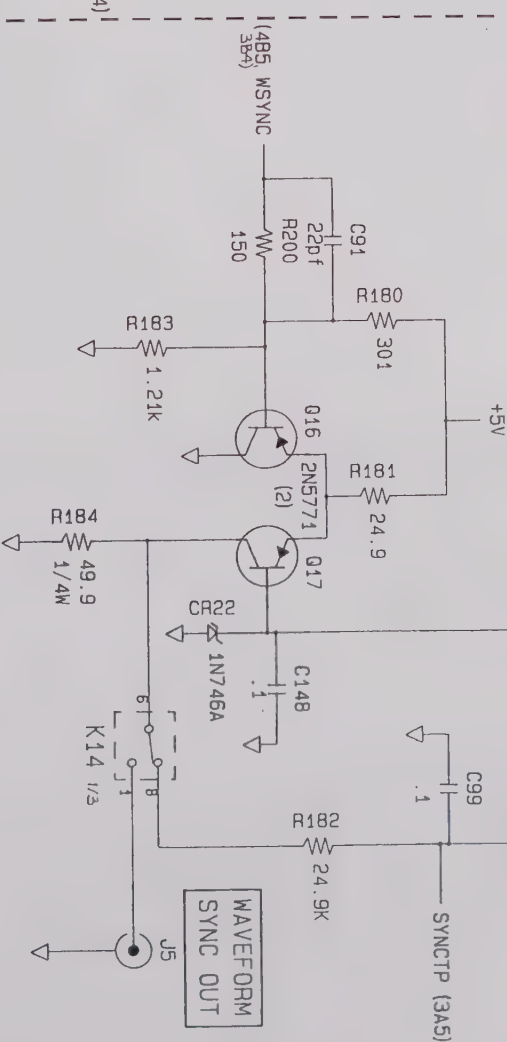
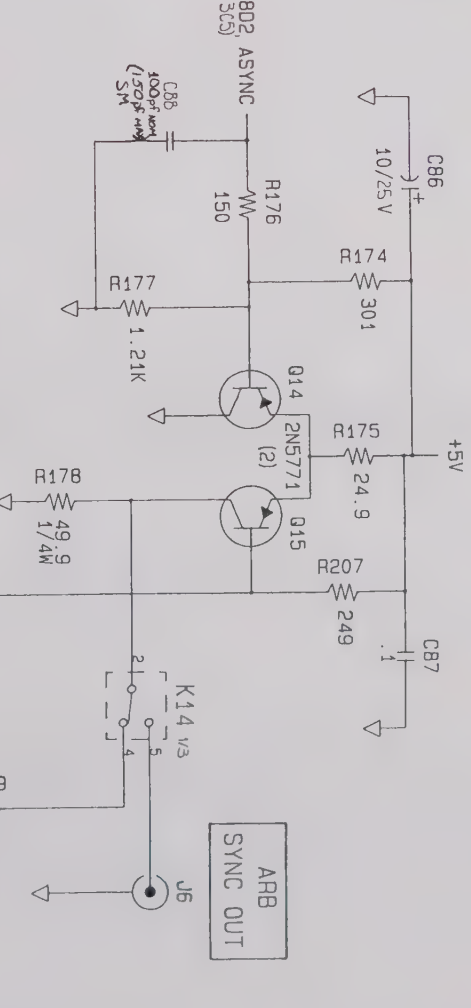
SCALE 2:3338

REMOVE ALL BURNS AND BREAK SHARP EDGES MATERIAL
PROTECTIVE
RELEASE
TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX - .00 ANGLES 1:1
DO NOT SCALE DIMS
FINISH
WAVEJET PROCESS

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION
AND IS THE PROPERTY OF WAVE TEK. IT IS TO BE
REPRODUCED FOR ANY REASON EXCEPT CALIBRATION,
OPERATION, AND MAINTENANCE WITHOUT WRITTEN AU-
THORIZATION.



REF DES	PART#	QTY (USED)	GATE & PIN NUMBER
U14	74F00	1	12 13 11
U13	74ALS1035	3	9 8 11 10 12
U17	74ALS003	1	7 10
U3	74ALS174	1	4 5 3 2 1 9 8 7 6 10 11 12
U4	74ALS243	1	16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1



SUMMING AMPLIFIER

NOTE: UNLESS OTHERWISE SPECIFIED

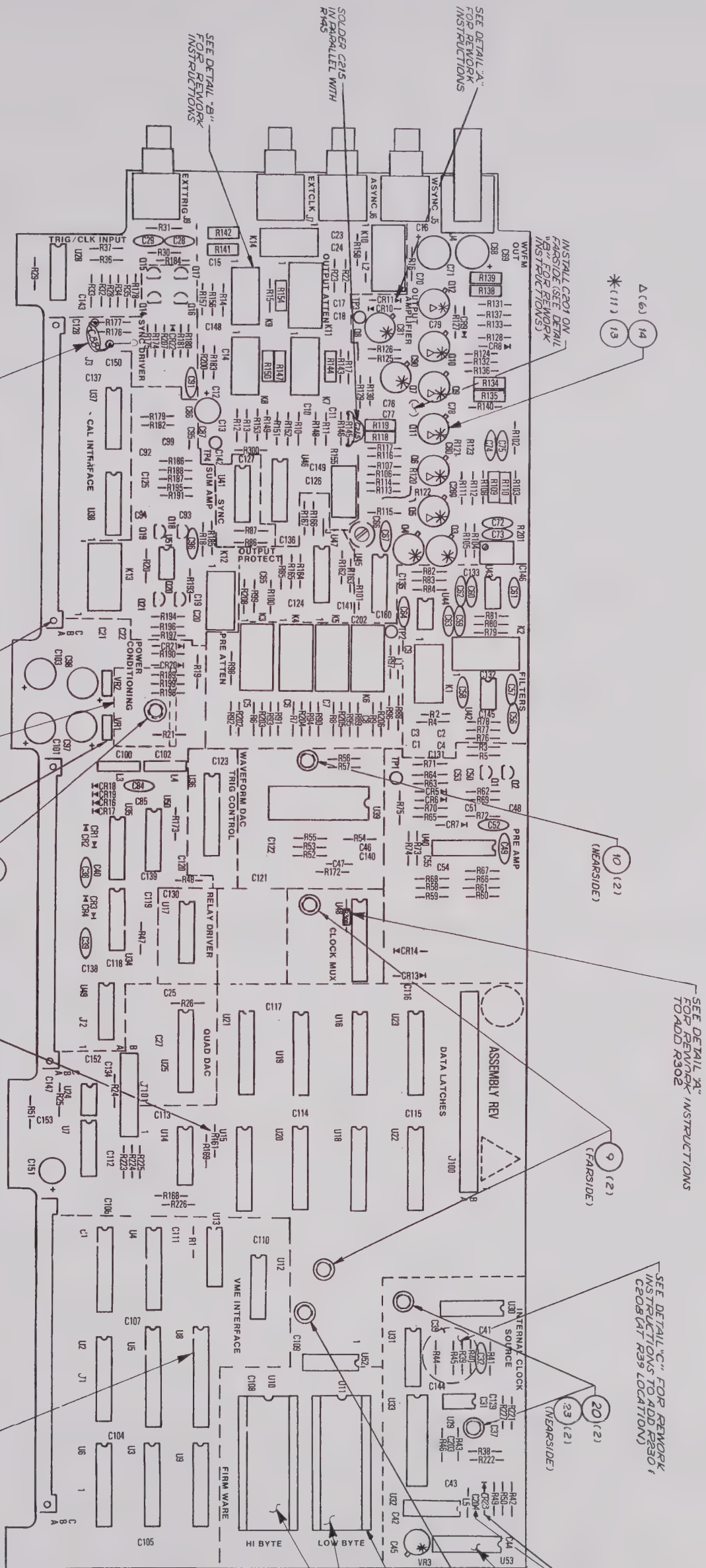
12 VOLT SUPPLIES

SCHEMATIC ARB GENERATOR

SIZE	FIG. NO.	DWG. NO.	REV.
D	2339A	1104-00-3281	A

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVEJET AND MAY NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT WRITTEN PERMISSION.

REV	ECO	BY	DATE	APP
A	ECO # 84-483	MS	3/4/81	11/81
B	ECO # 84-487	MS	6/81	5/82
C	ECO # 84-748	MS	4/81	8/82



CAUTION!
ALL REMOVAL ADDITIONS MUST NOT EXCEED HEIGHT OF ITEMS TO OR 20 (STANDOFFS) AFTER INSTALLATION.

PART NUMBER WAS-1100-00-3175

REVIEW ALL UNITS AND BREAK SHARD DOGS		DATE	
MATERIAL	CHECKED	7/1/81	7/1/81
DESIGN	CHECKED	7/1/81	7/1/81
WAVEJET PROCESS	CHECKED	7/1/81	7/1/81
UNLESS OTHERWISE SPECIFIED TOLERANCES ARE IN INCHES		UNLESS OTHERWISE SPECIFIED TOLERANCES ARE IN INCHES	
DO NOT SCALE DRAWING	SCALE 1/25:1	MODEL 680	SHEET 1 OF 3
WAVEJET		ASSEMBLY, ARB GEN BD.	
SIZE FROM NO. 2338		OWN NO. 1101-00-3281	REV C

ADD R255 TO U46 PIN 12 AND U41 PIN 11
ADD R254 TO U41 PINS 7 & 11
(SEE ADDENDUM, SHEET 3)

CUT TRACE AT
U41 PIN 11
(SEE ADDENDUM,
SHEET 3)

ADD CAP C217
BETWEEN PINS
517 OF U28 - KEEP
LEADS SHORT ~

BUSS U53 PINS 1 & 16
JUMPER DIK1 TO R42
(AS SHOWN)

ADD JUMPER WIRE
BETWEEN U52 PIN B
AND U53 PIN B

CUT TRACE

ADD CAP C255

ADD C253 TO U41 PIN 12
AND U46 PINS 7 & 11
(SEE ADDENDUM, SHEET 3)

K10 PIN 1 (SOLDER SIDE)

SOLDER ONE
LEAD OF R250
TO GND LEAD OF
C25

ROUTE SLEEVED WIRE THRU
MTG. HOLE OF U8 AND SOLDER
TO PIN 1 OF K10 (ON SOLDER
SIDE)

DETAIL "B"
REWORK INSTRUCTIONS
SOLDER SIDE

ADD C254 TO
U41 PINS 11 & 14
(SEE ADDENDUM,
SHEET 3)

CUT TRACE AT
H9 PIN 6

SEE SHEET 3
FOR MORE
INFORMATION

ADD R252 BETWEEN PINS
AND GND OF K12

INSTALL COAX CABLE (APPROX
1 1/2" LENGTH) BETWEEN ANODE
OF CP11 AND PIN 6 OF K9
SOLDER SHIELD TO GND AS SHOWN

HEATSINK
(PIN 400-02-3163)

R250 "MATCHED SET" SOLDER TOGETHER
IN PARALLEL BOND TO UNDERSIDE OF
HEATSINK WITH "REPAIRABLE THERMAL
ADHESIVE"

COMPONENT
SIDE (SHOWN
FOR CLARITY
ONLY)

ADD R302 BETWEEN TWO FEEDTHRUS
(AS SHOWN)

ADD C209 BETWEEN
PINS 12 & 18 OF U53
(LAY FLAT ON U53)

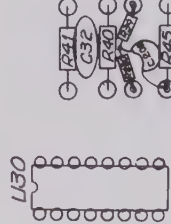
CUT TRACE AT
ANODE OF CP11

LIFT LEADS OF C28 (C29
AS SHOWN), ADD LEADS OF
R251 & R252 IN CAP HOLES,
AND SOLDER OPPOSITE ENDS
OF RES TO LIFTED CAP LEADS

DETAIL "A"
REWORK INSTRUCTIONS
COMPONENT SIDE

ADD CAP C251 BETWEEN PINS
11 & 11 OF U28, ADD CAP C252
BETWEEN PIN 12 OF U28 AND
GND LEAD OF C143

ADD JUMPER FROM
R161 TO FEEDTHRU
(AS SHOWN)



DETAIL "C"

SCALE: NONE

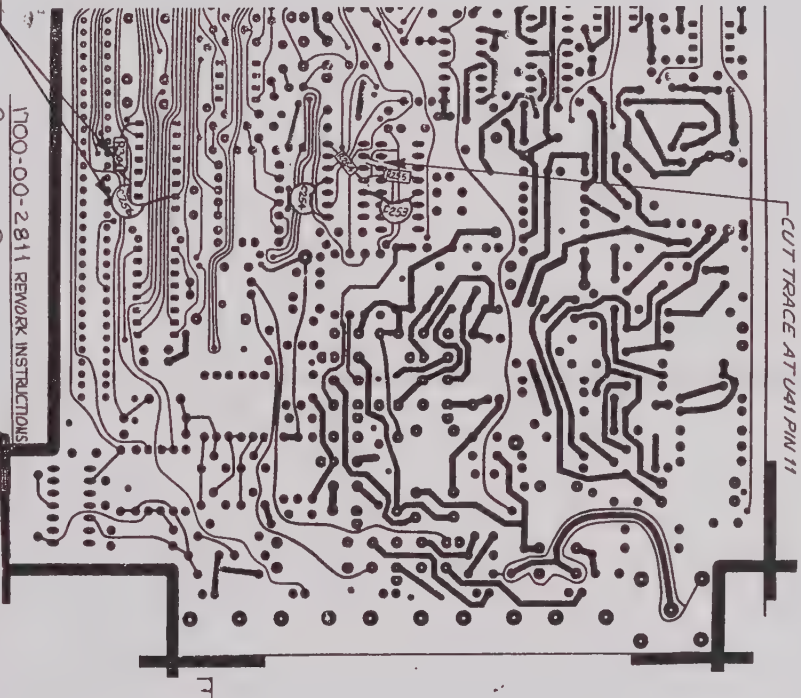
R230 & C208 INSTALLATION.
LIFT LEAD OF R39, INSERT ONE END
OF R230, SOLDER ONE LEAD OF C208
TO GND LEAD OF R45. SOLDER OPPOSITE
LEADS OF R230 & C208 TO LIFTED LEAD OF
R39

WAVEJET LASER BEAM & CALIBRATION	DATE 11/1/87	REV C
TITLE ASSEMBLY ARB GEN BD	SIZE D 23338	SCALE 1/101-00-3281
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES FRACTIONS DECIMALS ANGLES	1 2 3 4 5 6 7 8	1 2 3
DO NOT SCALE DRAWING	2	3

THIS DOCUMENT CONTAINS PROPRIETARY INFOR-
MATION. IT IS THE PROPERTY OF WAVE-
TEK AND IS NOT TO BE REPRODUCED FOR ANY
REASON EXCEPT CALIBRATION, OPERATION, AND
MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

SEE SHT #1

REV	ECN	BY	DATE	APP
-----	-----	----	------	-----



ADD SERIES RC BETWEEN
U38-8 AND U38-15
(R301, C250)

1100-00-2811 REMWORK INSTRUCTIONS
— SOLDER SIDE —
(EXPLODED REMWORK VIEW)
OF U41 MODIFICATIONS
ADDENDUM TO SHEET 2 of 1100-00-2811

1. ADD C253 BETWEEN U41 PIN 12 AND U46 PIN 13
2. ADD C254 TO PINS 1 & 4 OF U41
3. ADD R254 TO PINS 7 & 11 OF U41
4. ADD R255 TO U41 PIN 11 AND U46 PIN 12

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES		GRAPH M/S 1/1/89	DATE 7/1/89
MATERIAL		PROLENGTH	
FINISH WAVE TEK PROCESS		RELEASE METHOD	
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : .010 ANGLES : 1° XX : .030		DO NOT SCALE DWG	
SCALE	MODEL NO 680	DWG NO 1101-00-3281	REV C
3000 10001	23338	SHEET 3 OF 3	

ASSEMBLY
ARB GEN BD.

WAVE TEK
4440 N. 10TH ST. - CALIFORNIA

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFR-PART-NO	MFR	WAVETEK NO.	QTY/PT
R255	RES,SPACE HIBER, 1/3W, 1X, 1.1K	5063J01101F	NEPCO	0615-01101	1
R254	RES,SPACE HIBER, 1/3W, 1X, 750 OHM	5063J07500F	NEPCO	0615-07500	1
NONE	ABSY DRAINING, 20MHZ ARB MEM-MATE 1/F	1101-00-3281	WVTK	1101-00-3281	1
NONE	SCHEMATIC, 20MHZ ARB MEM-MATE 1/F	1104-00-3281	WVTK	1104-00-3281	1
26	HEATSINK, VR1 & VR2, ARB	1400-02-2623	WVTK	1400-02-2623	1
NONE	SHIELD, ARB	1400-02-2773	WVTK	1400-02-2773	1
30	MTG BRKT, XISTOR HEATSINK-ARB	1400-02-3143	WVTK	1400-02-3143	1
31	PLATE, XISTOR HEATSINK-ARB	1400-02-3153	WVTK	1400-02-3153	1
L3	L: FXD 2.2 OHM +/-10% MINI.	1025-28	DELON	130.9221	1
C251 C252	CAP, CER, 5PF, 1KV	DD-050 LONG LEAD	CHL	1500-00-5001	2
C28 C29	CAP, CER DISK, 5PF, 1KV, 10X	0311-00018	WVTK	1500-00-5011	2
C201 C215 C255 C68 C90	CAP, CER, 100PF, 1KV	DD-101	CHL	1500-01-0111	5

WAVETEK PARTS LIST

TITLE
PCA, 20MHZ ARB MEM BD-MATE 1/F

ASSEMBLY NO. 1100-00-3281

PAGE 1

REV E

ASSEMBLY NO. 1100-00-3281

PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFR-PART-NO	MFR	WAVETEK NO.	QTY/PT
C91	DISK, 1.5PF, 1KV, TEMP COMP	BD-220	CHL	1500-02-2011	1
C74 C75 C76 C77	CAP, CER, 22PF, 1KV	BD-221	CHL	1500-02-2111	4
C254	CAP, CER, 220PF, 1KV	CD287DMP0	ARCD	1500-02-7505	1
C256 C96	CAP, CER MON 2.7PF 50V	30A033	BPRAG	1500-03-3001	2
C64	CAP, CER DISK, 33PF, 1KV, 10X	0005CD100D03	CDE	1500-11-0006	1
C60	CAP, MICA, 10PF, 500V, 1X	CD15-ED220F03	CDE	1500-12-2006	1
C57	CAP, MICA, 22PF, 500V, 1X	CD15-ED240F03	CDE	1500-12-4006	1
C59	CAP, MICA, 24PF, 500V, 1X	DM15-241J	ARCD	1500-12-4100	1
C61	CAP, MICA, 240PF, 500V	DM15-301F	ARCD	1500-13-0101	1
C58	CAP, MICA, 300PF, 500V	DM15-331J	ARCD	1500-13-3100	1
C62 C63	CAP, MICA, 330PF, 500V	CD15-391J	CDE	1500-13-9100	2
C56	CAP, MICA, 91PF, 500V	DM15-910J	ARCD	1500-19-1000	1
C86	CAP, ELECT, 10MF/25V RADIAL LEAD, SP. 10	NRE 10/63	NIC	1500-31-0002	1
C101 C103 C151 C68 C71 C97 C98	CAP, ELECT, 100MF, 25V RADIAL LEAD, SP. 20	NRE101H35V10X12.5	NIC	1500-31-0102	7

WAVETEK PARTS LIST

TITLE
PCA, 20MHZ ARB MEM BD-MATE 1/F

ASSEMBLY NO. 1100-00-3281

PAGE 3

REV E

ASSEMBLY NO. 1100-00-3281

PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFR-PART-NO	MFR	WAVETEK NO.	QTY/PT
J101	CONN, 48 PIN DUAL ROM	2-333010-4	AMP	2100-02-0233	1
J1	CONN, DIN, MALE, 96 PIN, A/B/C, RTA	P196B30P00C00Z1	BURND	2100-02-0236	1
1	SOCKET, DUAL WIPE, 32 PIN	1CN-3268-SA-T	ROBNU	2100-03-0086	2
TP1 TP2 TP3 TP4	BUSS BAR STANDOFF	2110-001	ARTMR	2100-05-0024	4
10	STANDOFF, SHAGE .375 H. 250 HEX6-32. .062 MATL	1531B-3/B	USECO	2800-02-0002	2
20	STANDOFF, SHAGE .500 H. 250 HEX6-32. .062 MATL	1531B-1/2-11	USECO	2800-02-0003	2
12	STANDOFF, SHAGE .125 H. 250 DIA4-40. .062 MATL	9531B-0440-3A	ANTDM	2800-03-0004	1
9	STANDOFF, SHAGE .187L 250DIA, 4-40, KNURL	BR6911SP8-0, 187-34	LYNTR	2800-06-0018	2
13	TRANSIPAD	1012CN	METRS	2800-11-0003	11
14	HEATSINK, CUP CLIP, T05	260-4TH58	EGG-H	2800-11-0026	6
24	SCREW, 4-40X1/4, PHP, NY LOCK PATCH, Z 4-40X1/4	4-40 X 1/4	CHMCL	2800-23-4104	2

WAVETEK PARTS LIST

TITLE
PCA, 20MHZ ARB MEM BD-MATE 1/F

ASSEMBLY NO. 1100-00-3281

PAGE 5

REV E

ASSEMBLY NO. 1100-00-3281

PAGE 5

[illegible]

REMOVE ALL BURRS AND BREAK SHARP EDGES		DRAWN	DATE
MATERIAL		CHECKED	
		PROJ. ENG'R.	
		RELEASE APPROV	
FINISH WAVETEK PROCESS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX : XX :	
DO NOT SCALE DRAWING		SIZE FROM NO. D 23338	REV E
		1100-00-3281	
		MODEL 680-01	SHEET 1 OF 3

PARTS LIST
20 MHZ ARB

WAVETEK
SAN DIEGO • CALIFORNIA

REFERENCE DESIGNATORS	PART DESCRIPTION	DR10-WFGR-PART-NO	WFGR	WAVETEK NO.	QTY/PT
R10 R11 R111 R114 R12 R13 R132 R133 R136 R137 R14 R15 R16 R17 R18 R19 R2 R20 R21 R22 R23 R26 R3 R4 R49 R5 R30 R36 R37 R6 R7 R8 R9	RES, MF, 1/BM, 1X, 10	5043ED10R100F	TRM	4701-03-1009	33
R102 R103 R106 R107	RES, MF, 1/BM, 1X, 1, 1K	RM35D-1101F	TRM	4701-03-1101	4
R76	RES, MF, 1/BM, 1X, 11K	RM35D-1102F	TRM	4701-03-1102	1
R177 R183	RES, MF, 1/BM, 1X, 1, 21K	RM35D-1211F	TRM	4701-03-1211	2
R81	RES, MF, 1/BM, 1X, 124	RM35D-1240F	TRM	4701-03-1240	1
R38 R39	RES, MF, 1/BM, 1X, 140	RM35D-1400F	TRM	4701-03-1400	2
R176 R200 R220 R84	RES, MF, 1/BM, 1X, 150	RM35D-1500F	TRM	4701-03-1500	4
R125 R126 R63 R70	RES, MF, 1/BM, 1X, 1, 3K	RM35D-1501F	TRM	4701-03-1501	4
R162 R165 R87	RES, MF, 1/BM, 1X, 15K	RM35D-1502F	TRM	4701-03-1502	3
R108 R117	RES, MF, 1/BM, 1X, 15	RM35D-1506F	TRM	4701-03-1509	2
R77	RES, MF, 1/BM, 1X, 17, 4K	RM35D-1742F	TRM	4701-03-1742	1
R194 R301 R42 R83	RES, MF, 1/BM, 1X, 200	RM35D-2000F	TRM	4701-03-2000	4
R28 R32 R54	RES, MF, 1/BM, 1X, 2K	RM35D-2001F	TRM	4701-03-2001	3
R112 R113 R207 R25	RES, MF, 1/BM, 1X, 249	RM35D-2490F	TRM	4701-03-2490	4
R128 R131 R187 R38	RES, MF, 1/BM, 1X, 2, 49K	RM35D-2491F	TRM	4701-03-2491	4

WAVETEK PARTS LIST	TITLE PCA, 20MHZ ARB MEN BD-WATE I/F	ASSEMBLY NO. 1100-00-3281	REV E
PAGE 7			

REFERENCE DESIGNATORS	PART DESCRIPTION	DR10-WFGR-PART-NO	WFGR	WAVETEK NO.	QTY/PT
R161	RES, MF, 1/BM, 1X, 46, 4K	RM35D-4642F	TRM	4701-03-4642	1
R78	RES, MF, 1/BM, 1X, 4, 75K	RM35D-4731F	TRM	4701-03-4731	1
R221 R222 R46 R68 R86	RES, MF, 1/B, 1X, 499	RM35D-4990F	TRM	4701-03-4990	5
R30 R31	RES, MF, 1/BM, 1X, 4, 99K	RM35D-4991F	TRM	4701-03-4991	2
R136	RES, MF, 1/BM, 1X, 4, 99K	RM35D-4992F	TRM	4701-03-4992	1
R145	RES, MF, 1/BM, 1X, 54, 9	RM35D-5489F	TRM	4701-03-5489	1
R185	RES, MF, 1/BM, 1X, 576	RM35D-5760F	TRM	4701-03-5760	1
R64 R71	RES, MF, 1/BM, 1X, 604	RM35D-6040F	TRM	4701-03-6040	2
R131 R152 R186 R188	RES, MF, 1/BM, 1X, 619	RM35D-6190F	TRM	4701-03-6190	4
R302 R82	RES, MF, 1/BM, 1X, 61, 9	RM35D-6199F	TRM	4701-03-6199	2
R230 R39	RES, MF, 1/BM, 1X, 6, 81K	RM35D-6811F	TRM	4701-03-6811	2
R146	RES, MF, 1/BM, 1X, 69, 8	RM35D-6988F	TRM	4701-03-6989	1
R43	RES, MF, 1/BM, 1X, 7, 32K	RM35D-7321F	WVTK	4701-03-7321	1
R129 R130 R168 R169	RES, MF, 1/BM, 1X, 750	RM35D-7500F	TRM	4701-03-7500	4
R60 R61	RES, MF, 1/BM, 1X, 7, 3K	RM35D-7501F	TRM	4701-03-7501	2
R40	RES, MF, 1/BM, 1X, 7, 87K	RM35D-7871F	TRM	4701-03-7871	1
R35	RES, MF, 1/BM, 1X, 8, 25K	RM35D-8231F	TRM	4701-03-8231	1

WAVETEK PARTS LIST	TITLE PCA, 20MHZ ARB MEN BD-WATE I/F	ASSEMBLY NO. 1100-00-3281	REV E
PAGE 9			

REFERENCE DESIGNATORS	PART DESCRIPTION	DR10-WFGR-PART-NO	WFGR	WAVETEK NO.	QTY/PT
CR23	CONDUCTANCE, ULTRA FAST	WV1404	NOT	4803-02-1404	1
CR13 CR14 CR20 CR21 CR3 CR6	DIODE, HIGH CAP TUNING	1M4148	FAIR	4807-02-4444	6
CR1 CR16 CR17 CR18 CR19 CR2	COMPUTER, C/P, 75V, 200M A, SWITCHING	5082-2811	HP	4809-02-2811	8
CR3 CR4	TRANS 2M2219A NPN	2M2219A	NSC	4901-02-2191	2
CR3 CR8	TRANS 2M2304A PNP	2M2304A	NSC	4901-02-7051	2
CR4 CR7	TRANS 2M2304A NPN	2M2304A	NOT	4901-02-6640	3
CR10 CR12 CR5	TRANS 2M3904 NPN	2M3904	FAIR	4901-02-7040	2
CR18 CR21	TRANS 2M3906 PNP	2M3906	FAIR	4901-02-7040	2
CR19 CR20	TRANS 2M3771 PNP	2M3771	NOT	4901-02-1600	3
CR11 CR6 CR9	TRANS 2M3771 PNP	2M3771	NSC	4901-02-7710	4
CR10 CR15 CR16 CR17 CR2	ANALOG SWITCH, CMOS	DS243CJ	BLCON	7000-02-4300	1

WAVETEK PARTS LIST	TITLE PCA, 20MHZ ARB MEN BD-WATE I/F	ASSEMBLY NO. 1100-00-3281	REV E
PAGE 11			

REFERENCE DESIGNATORS	PART DESCRIPTION	DR10-WFGR-PART-NO	WFGR	WAVETEK NO.	QTY/PT
R179 R182 R198 R199	RES, MF, 1/BM, 1X, 24, 9K	RM35D-2492F	TRM	4701-03-2492	4
R173 R181	RES, MF, 1/BM, 1X, 24, 9	RM35D-2499F	TRM	4701-03-2499	2
R80	RES, MF, 1/BM, 1X, 287	RM35C2870F	DALE	4701-03-2870	1
R33	RES, MF, 1/BM, 1X, 2, 87K	RM35D-2871F	TRM	4701-03-2871	1
R174 R180 R193	RES, MF, 1/BM, 1X, 301	RM35D-3010F	TRM	4701-03-3010	3
R133 R251 R232	RES, MF, 1/BM, 1X, 3, 01K	RM35D-3011F	TRM	4701-03-3011	3
R140	RES, MF, 1/BM, 1X, 301K	RM35D-3013F	TRM	4701-03-3013	1
R191 R195 R98	RES, MF, 1/BM, 1X, 332	RM35D-3320F	TRM	4701-03-3320	3
R62 R69	RES, MF, 1/BM, 1X, 3, 32K	RM35D-3321F	TRM	4701-03-3321	2
R167 R32	RES, MF, 1/BM, 1X, 33, 2K	RM35D-3322F	TRM	4701-03-3322	2
R101 R173 R189 R190 R47	RES, MF, 1/BM, 1X, 392	RM35D-3920F	TRM	4701-03-3920	5
R34 R35	RES, MF, 1/BM, 1X, 3, 92K	RM35D-3921F	TRM	4701-03-3921	2
R36 R37	RES, MF, 1/BM, 1X, 4, 02K	RM35D-4021F	TRM	4701-03-4021	2
R148 R29 R33	RES, MF, 1/BM, 1X, 40, 2K	RM35D-4022F	TRM	4701-03-4022	3
R100 R104 R105	RES, MF, 1/BM, 1X, 432	RM35D-4320F	TRM	4701-03-4320	3
R83	RES, MF, 1/BM, 1X, 453	RM35D-4530	TRM	4701-03-4530	1

WAVETEK PARTS LIST	TITLE PCA, 20MHZ ARB MEN BD-WATE I/F	ASSEMBLY NO. 1100-00-3281	REV E
PAGE 8			

REFERENCE DESIGNATORS	PART DESCRIPTION	DR10-WFGR-PART-NO	WFGR	WAVETEK NO.	QTY/PT
R113 R116	RES, MF, 1/BM, 1X, 976	RM35D-9760F	TRM	4701-03-9760	2
R178 R184	RES, MF, 1/4M, 1X, 49, 9	RM60D-4989F	TRM	4701-13-4999	2
R141 R130 R134	RES, MF, 1M, 2M, 1X, 50	MS22050, 1X2M	CADD0	4701-42-5009	3
R142	RES, MF, 1M, 2M, 1X, 61, 1, SIZE 4L	MS220, 61, 1, 1X, 2M, MF	CADD0	4701-42-6119	1
R135	RES, MF, 1M, 3M, 1X, 61, 9, SIZE 4BL	MS223, 61, 9, 1X, 3M, MF	CADD0	4701-52-6199	1
R230	RES, MATCHED SET 50 OHM 1X, 13M	4789-00-0053	WVTK	4789-00-0053	1
R144 R147	RES, MF, 2M, 1X, 249	MS220-249	CADD0	4799-00-0145	2
R134 R135 R138 R139	RES, MF, 2M, 1X, 73	MS220-73	CADD0	4799-00-0131	4
R120 R121 R122 R123	RES, MF, 75M, 1X, 50	MS132-50	CADD0	4799-00-0132	4
CR22	DIODE, ZENER, 3, 3V, 5% TOL, 500MA, 0/8, IN7464	IN7464	FAIR	4801-01-0746	1
CR7	DIODE, ZENER, 5, 1V, 500MA, 618, IN751A	IN751A	FAIR	4801-01-0751	1
CR8 CR9	DIODE, ZENER, 10V, CLASS BILICOM, 1M	1M4740A	NOT	4801-01-4740	2
CR10 CR11	DIODE, 1M10H	1M5282	FAIR	4801-01-5282	2

WAVETEK PARTS LIST	TITLE PCA, 20MHZ ARB MEN BD-WATE I/F	ASSEMBLY NO. 1100-00-3281	REV E
PAGE 10			

REFERENCE DESIGNATORS	PART DESCRIPTION	DR10-WFGR-PART-NO	WFGR	WAVETEK NO.	QTY/PT
U47	COMPARATORS, QUAD VOLTAGE	0665-00364	WVTK	7000-03-3900	1
U42	OP-AMP	LF354N	NSC	7000-03-5400	1
U37	MUX, CMOS, 8 CH, B CHAN/DUAL, 4 CHAN ANAL	DS3084NCJ	BLCON	7000-03-0800	1
U28 U41	COMPARATOR, DUAL DIFFERENTIAL, SENSE AMP	NE521	SL6	7000-03-2100	2
U24 U29	OP AMP INPUT	TL082CP	TI	7000-08-2000	2
U17	DARLINGTON ARRAYS, HIGH VOLTAGE, HIGH CURRENT	ULN2003A	SPRAO	7000-20-0300	1
U43	OP-AMP, LIN, WIDE BAND	HA418	FAIR	7000-25-4000	1
U40	TRANS ARRAY, GENERAL PURPOSE, NPN	CA3083	FAIR	7000-30-6300	1
U43 U44 U51	VIDEO BUFFER	HA3-5033-5	HA818	7000-50-3300	3
U41	VOLT REGULATOR, POSITIVE	MC7812CT	NOT	7000-78-1200	1
U42	VOLT REGULATOR, NEGATIVE	7912	NOT	7000-79-1200	1

WAVETEK PARTS LIST	TITLE PCA, 20MHZ ARB MEN BD-WATE I/F	ASSEMBLY NO. 1100-00-3281	REV E
PAGE 12			

REMOVE ALL BURNS AND BREAK SHARP EDGES

DATE

WAVETEK

20 MHZ ARB

23338

1100-00-3281

680-01

2

3

SCALE

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. TOLERANCES ARE FRACTIONS, DECIMALS, AND MILLIMETERS.

REV

DATE

APP

D

REFERENCE DESIGNATORS	PART DESCRIPTION	DR10-MFOR-PART-NO	MFOR	WAVETEK NO.	QTY/PT	REFERENCE DESIGNATORS	PART DESCRIPTION	DR10-MFOR-PART-NO	MFOR	WAVETEK NO.	QTY/PT
U39	DMC, 12 BIT, 20MHZ	TDC1012N7-C2	TRW	8000-10-1200	1	U10	EPROM, PROG SET, 1 EA 8002-75-1200 FOR MFD 6800 ARB, V1.0, 7 REF U11	8600-00-0578	WAVET	8600-00-0578	1
U25	DMC, GUAD 8-BIT	A07226-JN	ANDEV	8000-72-2600	1	U23	ARRAY, GATE, SPEED GRADED DMC 2016-3	8700-00-0002	WVTK	8700-00-0005	1
U14	GATE, NAND, GUAD 21NF, TTL	74F00PC	FAIR	8000-74-0002	1						
U31	FLIP-FLOP DUAL, D-POS EDGE TRIG, TTL	74LS74	TI	8000-74-7410	1						
VR3	VOLT REGULATOR	UA78M03HC	FAIR	8000-78-0501	1						
U35	TRANSLATOR, GUAD TTL-TO-MECL	MC10H124P	MDT	8001-01-2401	1						
U34 U50	TRANSLATOR, GUAD TTL-TO-MECL	MC10H125P	MDT	8001-01-2501	2						
U53	TRANSLATOR, ECL TO TTL	MC10H350P	MDT	8001-03-5000	1						
U12	DECODER, DUAL 2-4, TTL	74LS139	SIG	8007-41-3910	1						
U38	DATA SELECTOR/MUX, ADV LD PUR SCHOTTKY, 16-PIN DIP	SN74ALS151N/J	MDT	8007-41-5111	1						
U52	SHIFT REG 8B SISO, TTL	74LS164	TI	8007-41-6410	1						
U1 U2 U4	BUF/ALN DRIVER, OCTAL W/3 STATE	SN74ALS541N	TI	8007-45-4100	3						
WAVETEK PARTS LIST		TITLE PCA, 20MHZ ARB MEM BD-MATE I/F		ASSEMBLY NO. 1100-00-3281		WAVETEK PARTS LIST		TITLE PCA, 20MHZ ARB MEM BD-MATE I/F		ASSEMBLY NO. 1100-00-3281	
				PAGE 13						PAGE 15	
				REV E						REV E	

C

WAVETEK PARTS LIST		TITLE PCA, 20MHZ ARB MEM BD-MATE I/F		ASSEMBLY NO. 1100-00-3281		REV E	
				PAGE 14			

REFERENCE DESIGNATORS	PART DESCRIPTION	DR10-MFOR-PART-NO	MFOR	WAVETEK NO.	QTY/PT	REFERENCE DESIGNATORS	PART DESCRIPTION	DR10-MFOR-PART-NO	MFOR	WAVETEK NO.	QTY/PT
U19 U16 U18 U19 U20 U21	FLIP-FLOP, OCTAL D	SN74ALS74N	TI	8007-45-7450	6	U19 U16 U18 U19 U20 U21	FLIP-FLOP, OCTAL D	SN74ALS74N	TI	8007-45-7450	6
U22 U23 U3 U6 U9	TRANSCIEVER, OCTAL BUS W/3 STATE	SN74ALS645A-1N	TI	8007-46-4500	5	U22 U23 U3 U6 U9	TRANSCIEVER, OCTAL BUS W/3 STATE	SN74ALS645A-1N	TI	8007-46-4500	5
U7	GATE XOR GUAD	74F86PC	FAIR	8007-48-6000	1	U7	GATE XOR GUAD	74F86PC	FAIR	8007-48-6000	1
U30	PLL	MC145157P2	MDT	8014-51-5700	1	U30	PLL	MC145157P2	MDT	8014-51-5700	1
U13 U49	BUFF, HEX NONINVERT W/OC	SN74ALS1035N	TI	8074-10-3500	2	U13 U49	BUFF, HEX NONINVERT W/OC	SN74ALS1035N	TI	8074-10-3500	2
U32	DBC ENT CUPLD, ECL	MC1648P	MDT	8100-16-4810	1	U32	DBC ENT CUPLD, ECL	MC1648P	MDT	8100-16-4810	1
U8	PAL, PROG, USES 1 EA 8000-20-4000 FOR MODEL 680 VER 1.2	8600-00-0458	WVTK	8600-00-0458	1	U8	PAL, PROG, USES 1 EA 8000-20-4000 FOR MODEL 680 VER 1.2	8600-00-0458	WVTK	8600-00-0458	1
U5	PAL, PROG, USES 1 EA 8000-20-8000 FOR MODEL 680 VER 1.0	8600-00-0459	WVTK	8600-00-0459	1	U5	PAL, PROG, USES 1 EA 8000-20-8000 FOR MODEL 680 VER 1.0	8600-00-0459	WVTK	8600-00-0459	1
U36	GAL, PROG, USES 1 EA 8000-16-8002 FOR MFD 680 ARB, V1.0, 7 REF	8600-00-0467	WVTK	8600-00-0467	1	U36	GAL, PROG, USES 1 EA 8000-16-8002 FOR MFD 680 ARB, V1.0, 7 REF	8600-00-0467	WVTK	8600-00-0467	1
U48	GAL, PROG, USES 1EA 8000-16-8002 FOR MDT 680 ARB V 2.0, REF U48	8600-00-0566	WVTK	8600-00-0566	1	U48	GAL, PROG, USES 1EA 8000-16-8002 FOR MDT 680 ARB V 2.0, REF U48	8600-00-0566	WVTK	8600-00-0566	1
U11	EPROM, PROG, SET, 1 EA 8002-75-1200 FOR MFD 680 ARB, V1.0, 7 REF U10	8600-00-0577	WAVET	8600-00-0577	1	U11	EPROM, PROG, SET, 1 EA 8002-75-1200 FOR MFD 680 ARB, V1.0, 7 REF U10	8600-00-0577	WAVET	8600-00-0577	1
WAVETEK PARTS LIST		TITLE PCA, 20MHZ ARB MEM BD-MATE I/F		ASSEMBLY NO. 1100-00-3281		WAVETEK PARTS LIST		TITLE PCA, 20MHZ ARB MEM BD-MATE I/F		ASSEMBLY NO. 1100-00-3281	
				PAGE 14						PAGE 15	
				REV E						REV E	

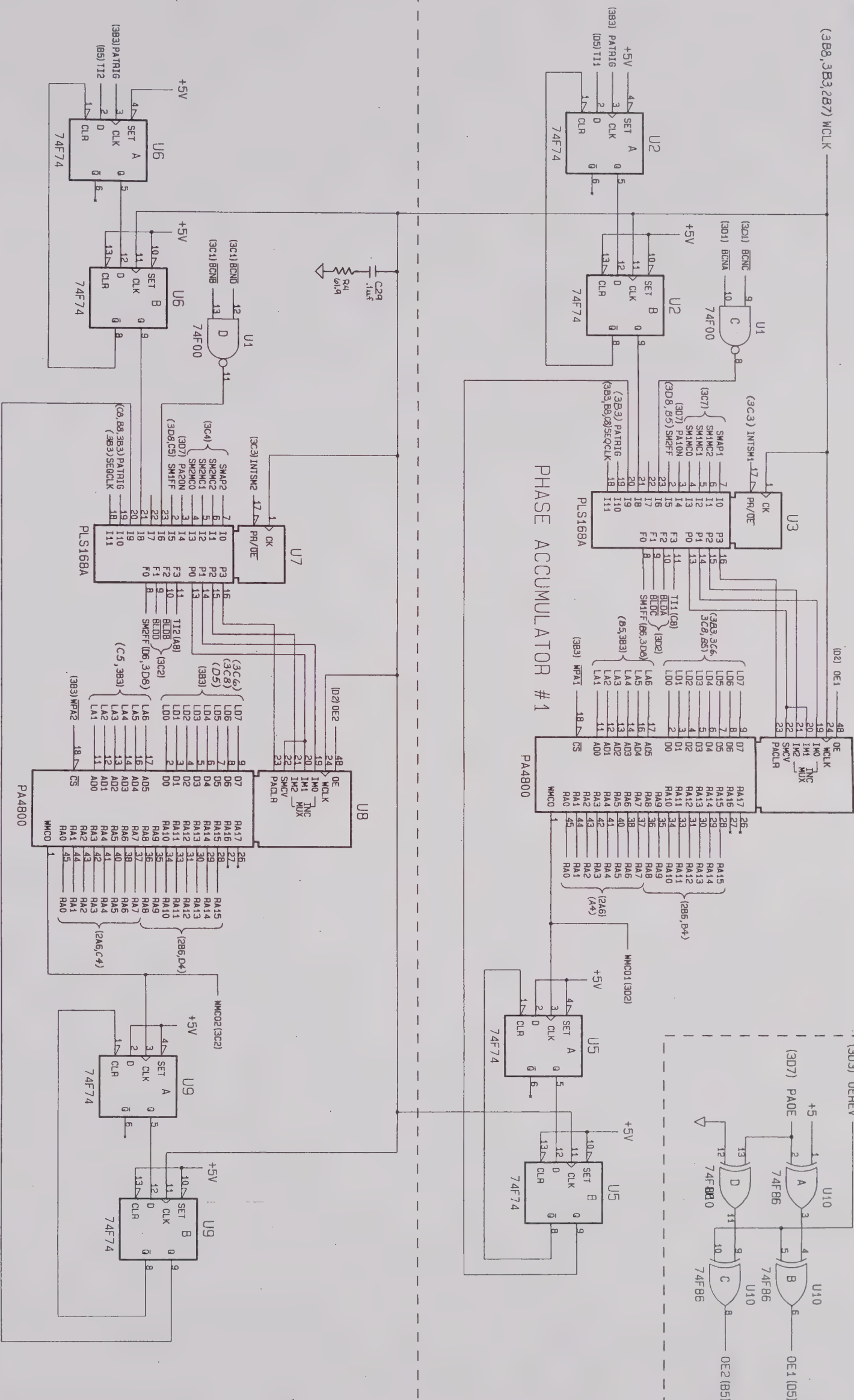
B

A

REMOVE ALL BURRS AND BREAK SHARP EDGES MATERIAL	DATE	DATE	DATE
CHECKED	CHECKED	CHECKED	CHECKED
PROJ ENG	PROJ ENG	PROJ ENG	PROJ ENG
RELEASE APPROV.	RELEASE APPROV.	RELEASE APPROV.	RELEASE APPROV.
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES	SIZE FROM NO. D 23338	REV E
DO NOT SCALE DRAWING	SCALE	MODEL 680-01	SHEET 3 OF 3

WAVETEK SAN DIEGO • CALIFORNIA	TITLE PARTS LIST 20 MHZ ARB	DATE 1100-00-3281	REV E
SCALE	MODEL 680-01	SHEET 3 OF 3	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO MICROTHERM CORPORATION. IT IS TO BE USED FOR RESEARCH AND DEVELOPMENT PURPOSES ONLY AND IS NOT TO BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT WRITTEN AUTHORIZATION.



PHASE ACCUMULATOR #2

PHASE ACCUMULATOR #1

2. ALL RESISTORS ARE IN OHMS
NOTE: UNLESS OTHERWISE SPECIFIED, ALL COMPONENTS ARE IN MICROAMPS

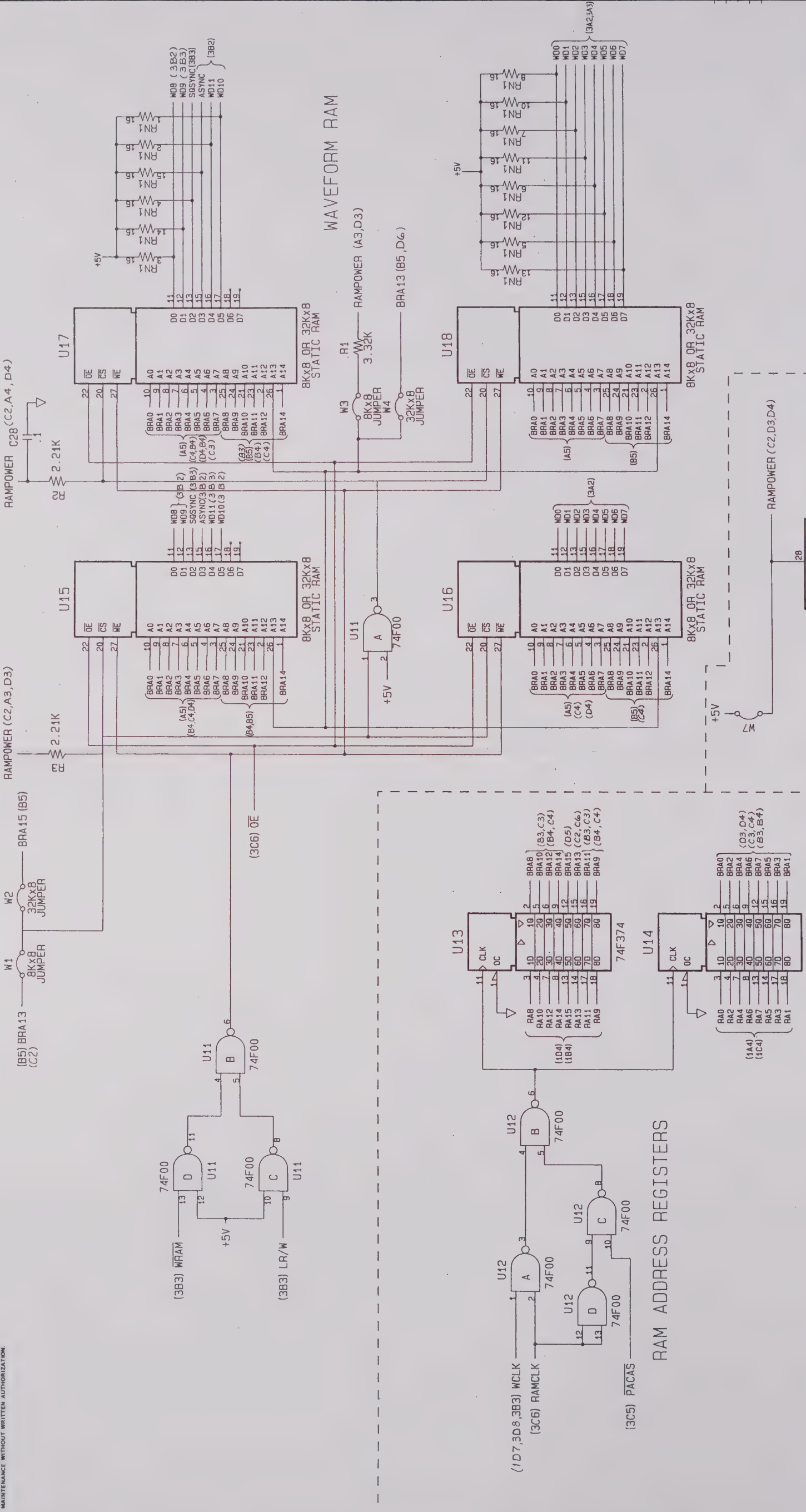
REV	ECN	BY	DATE	APP
A	ERO # 9755	Y/L	9/1/84	CE
B	ECO # 89-697	MS	9/1/84	CE

REMOVE ALL BURRS AND BREAK SHARP EDGES		DATE	6-80
MATERIAL		6-1/8	6-1/8
FINISH		XXX-300	XXX-300
WAVEFORM PROCESS		XXX-300	XXX-300
DO NOT SCALE DIMS		XXX-300	XXX-300
SCALE		XXX-300	XXX-300
MODEL NO.		680-001	0103-00-3129
CODE		23338	REV B
SHEET		1	OF 3

SCHEMATIC
ARB MEMORY

WAVETEK

WAVETEK	DATE: 6-7-88	TITLE: SCHEMATIC	REV: B
PROJECT: 680-001	DESIGNER: J. R. Rios	RELEASED: 6/1/88	MODEL NO. 680-001
REMOVE ALL BURRS AND BREAK SHARP EDGES MATERIAL		FINISH WAVETEK PROCESS	
TOLERANCE UNLESS OTHERWISE SPECIFIED XX ± .030 ANGLES 1:1		DO NOT SCALE DWG SCALE	
CODE: 23338		SHEET 2 OF 3	



WAVEFORM RAM

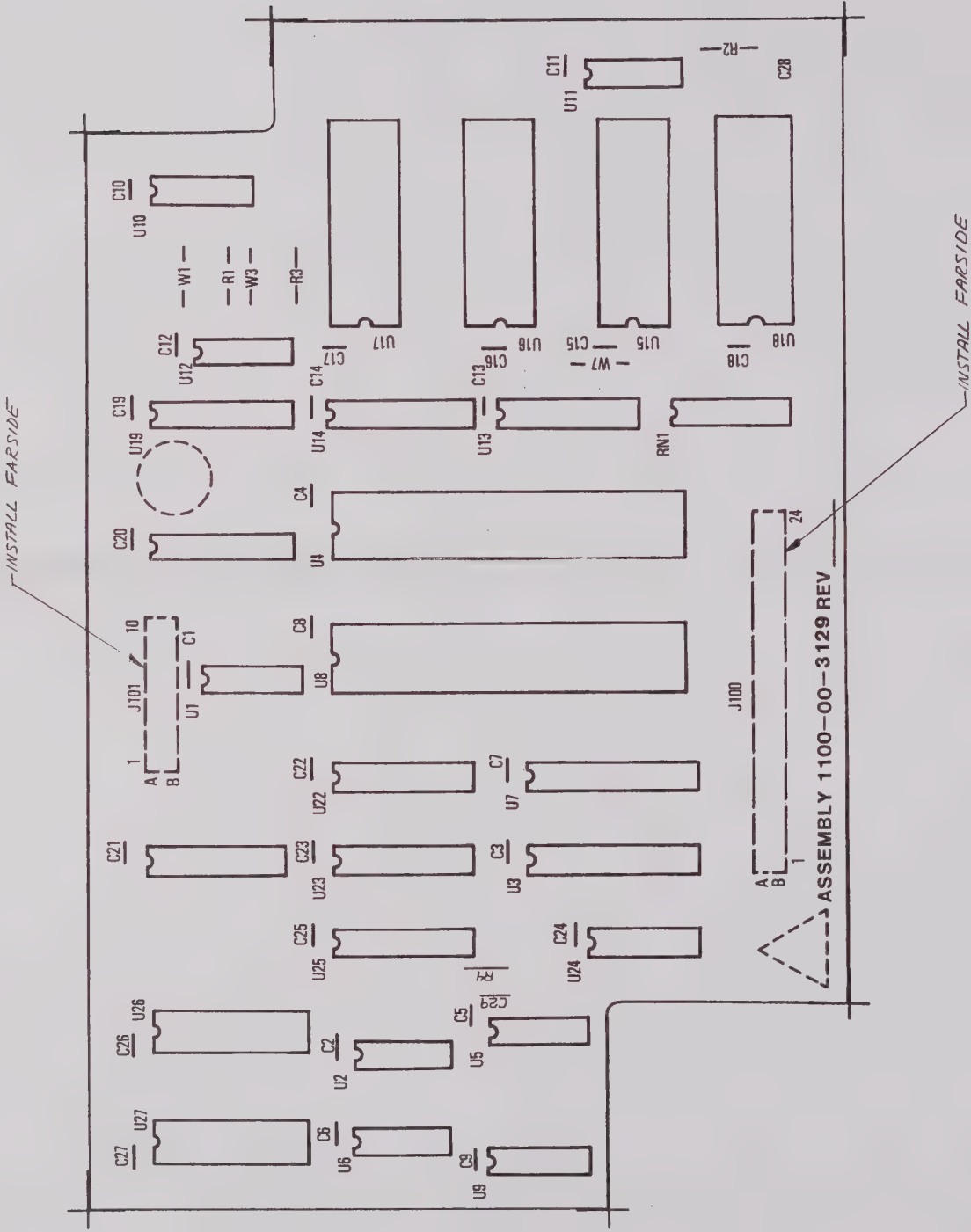
RAM ADDRESS REGISTERS

RAM POWER

U15-18
WAVEFORM
MEMORY
RAM

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVEJET CORPORATION. IT IS TO BE USED FOR REPAIR AND MAINTENANCE ONLY. REPRODUCTION OR TRANSMISSION OF THIS DOCUMENT WITHOUT WRITTEN AUTHORIZATION IS PROHIBITED.

REV	ECN	BY	DATE	APP
A	ERO# 9755	WJ	5/14/81	WJ
B	ECO# 9934	MS	10/1/81	WJ
C	ECO# 89-697	MS	10/1/81	WJ



WAVETEK SAN DIEGO - CALIFORNIA		DATE 10/1/81	
TITLE ARB MEMORY BOARD		DRAWN WJ	
DESIGNED WJ		CHECKED WJ	
MATERIAL —		FINISH WAVEJET PROCESS	
DO NOT SCALE DWG		SCALE	
MODEL NO 680		REV C	
SHEET 23338		OF 1	

NOTE UNLESS OTHERWISE SPECIFIED

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION
AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT
BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION,
OPERATION, AND MAINTENANCE WITHOUT WRITTEN AU-
THORIZATION.

NOTE: UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP
-----	-----	----	------	-----

REFERENCE DESIGNATORS	PART DESCRIPTION	ORI0-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, ARB MEMORY BD	0103-00-3129	WVTK	0103-00-3129	1
C1 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C2 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C3 C4 C5 C6 C7 C8 C9	CAP CER MON .1MF 50V 75U +80/-20% RAD LD SP .2 SP .2	BR215E1042AA	AVX	1500-01-0420	29
NONE	PCB, ARB GEN PGY BK BD REF: SPEC 0008-00-0455 REV C	1700-00-2876	WVTK	1700-00-2876	1
J100	CONN, DUAL 24 PIN-STRAIGHT	929665-01-24	APTRN	2100-02-0242	1
J101	CONN, HEADER, 20 PIN	929836-01-10	AP	2100-05-0042	1
R2 R3	RES, MF, 1/BW, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	2
R1	RES, MF, 1/BW, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	1
R4	RES, MF, 1/BW, 1%, 61.9	RN55D-61R9F	TRW	4701-03-6199	1
RN1	RES NETWORK, DUAL IN-LINE, 16 PIN, 1000 OHM	4116R-002-102	BOURN	4770-00-0061	1
W1 W3 W7	RES, 0 OHM JUMPER	JP02T680	ROHM	4799-00-0087	3
U1 U11 U12	GATE, NAND, QUAD 21NP, TTL	74F00PC	FAIR	8000-74-0002	3
U2 U5 U6 U9	FLIP-FLDP DUAL, D-POS	74F74PC	FAIR	8000-74-7402	4
WAVETEK PARTS LIST		TITLE PCA, ARB MEMORY BD			ASSEMBLY NO. 1100-00-3129
					REV C
					PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORI0-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U15 U16 U17 U18	EDGE TRI0, TTL				
U24	SRAM, 8KX8, 35NS, CMOS	CY7C186L-35PC	CYP	8007-18-4000	4
U13 U14	DECODER, 1-8 LINE, TTL	74LS138	TI	8007-41-3810	1
U22 U23 U25	FLIP-FLDP, OCTAL D	74F374PC	FAIR	8007-43-7460	2
U10	FLIP-FLDP, OCTAL D	SN74ALS574N	TI	8007-43-7450	3
U3 U7	GATE XOR QUAD	74FB6PC	FAIR	8007-48-6000	1
U19	PLS, PROG, USES 1 EA 8000-16-8001 FOR MODEL 680 VER 1.0	8600-00-0460	WVTK	8600-00-0460	2
U4 U8	PAL, PROG, USES 1 EA 8000-16-4000 FOR MODEL 680 VER 1.0	8600-00-0461	WVTK	8600-00-0461	1
U26 U27	QA, PHASE ACCUMULATOR-CUSTOM	PA4800	PLESS	8700-00-0001	2
	GATE ARRAY DNC 2016, USE 8700-00-0005	8700-00-0004	WVTK	8700-00-0002	2
WAVETEK PARTS LIST		TITLE PCA, ARB MEMORY BD			ASSEMBLY NO. 1100-00-3129
					REV C
					PAGE 2

REMOVE ALL BURRS AND BREAK SHARP EDGES		DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA TITLE PARTS LIST ARB MEMORY BD	
MATERIAL	CHECKED				
	PROJ. ENGR.				
	RELEASE APPROV.				
FINISH WAVETEK PROCESS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± .XXX ± .		SIZE D	FSCM NO. 23338
DO NOT SCALE DRAWING		SCALE		DWG. NO. 1100-00-3129	REV C
				MODEL 680-01	SHEET 1 OF 1

MP MASTER



MA25842